ST(意法) TDA7850 PDF

深圳创唯电子有限公司

http://www.st-ic.com

TDA7850

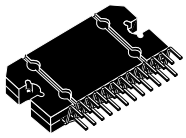
4 x 50 W MOSFET quad bridge power amplifier

Features

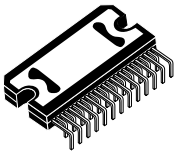
- High output power capability:
  - 4 x 50 W/4 Ω max.
  - 4 x 30 W/4 Ω @ 14.4 V, 1 kHz, 10 %
  - 4 x 80 W/2 Ω max.
  - 4 x 55 W/2 Ω @ 14.4V, 1 kHz, 10 %
- MOSFET output power stage
- Excellent 2 Ω driving capability
- Hi-Fi class distortion
- Low output noise
- ST-BY function
- Mute function
- Automute at min. supply voltage detection
- Low external component count:
  - Internally fixed gain (26 dB)
  - No external compensation
  - No bootstrap capacitors
- On board 0.35 A high side driver

Protections:

- Output short circuit to gnd, to V_S, across the load
- Very inductive loads
- Overrating chip temperature with soft thermal limiter
- Output DC offset detection
- Load dump voltage
- Fortuitous open gnd
- Reversed battery



Flexiwatt25 (Vertical)



Flexiwatt25 (Horizontal)

- ESD

Description

The TDA7850 is a breakthrough MOSFET technology class AB audio power amplifier in Flexiwatt 25 package designed for high power car radio. The fully complementary P-Channel/N-Channel output structure allows a rail to rail output voltage swing which, combined with high output current and minimized saturation losses sets new power references in the car-radio field, with unparalleled distortion performances.

The TDA7850 integrates a DC offset detector.

Table 1. Device summary

Order code	Package	Packing
TDA7850	Flexiwatt25 (Vertical)	Tube
TDA7850H	Flexiwatt25 (Horizontal	Tube

Contents

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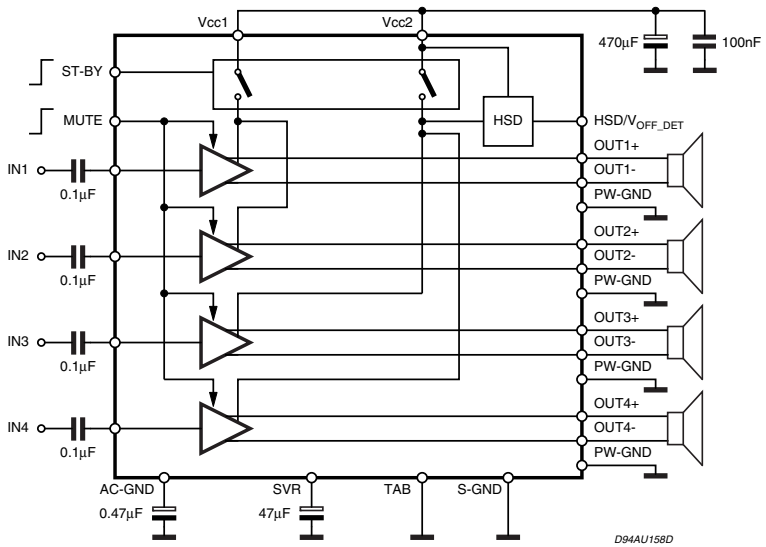
1 Block diagram and application circuit

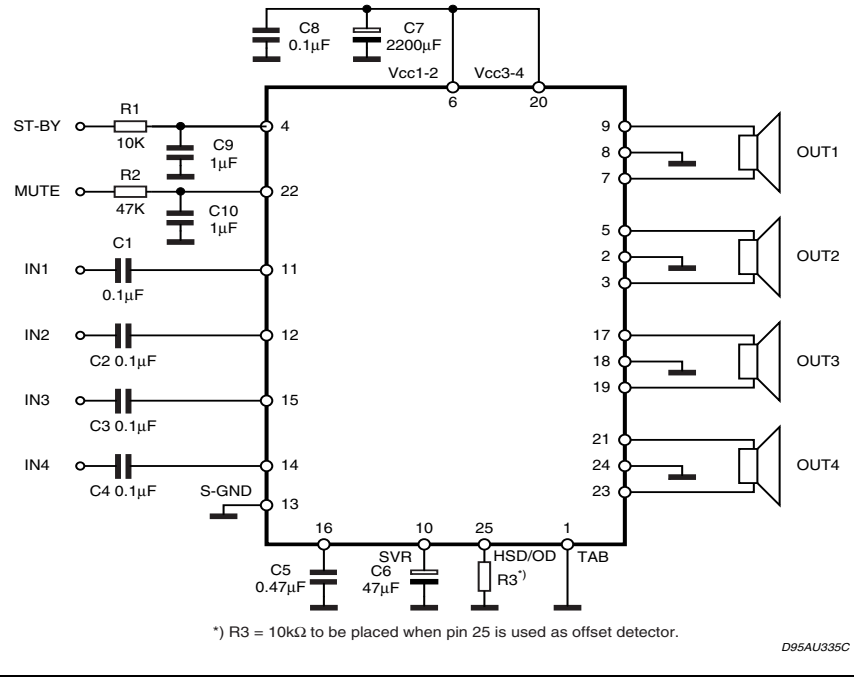
1.1 Block diagram

Figure 1. Block diagram



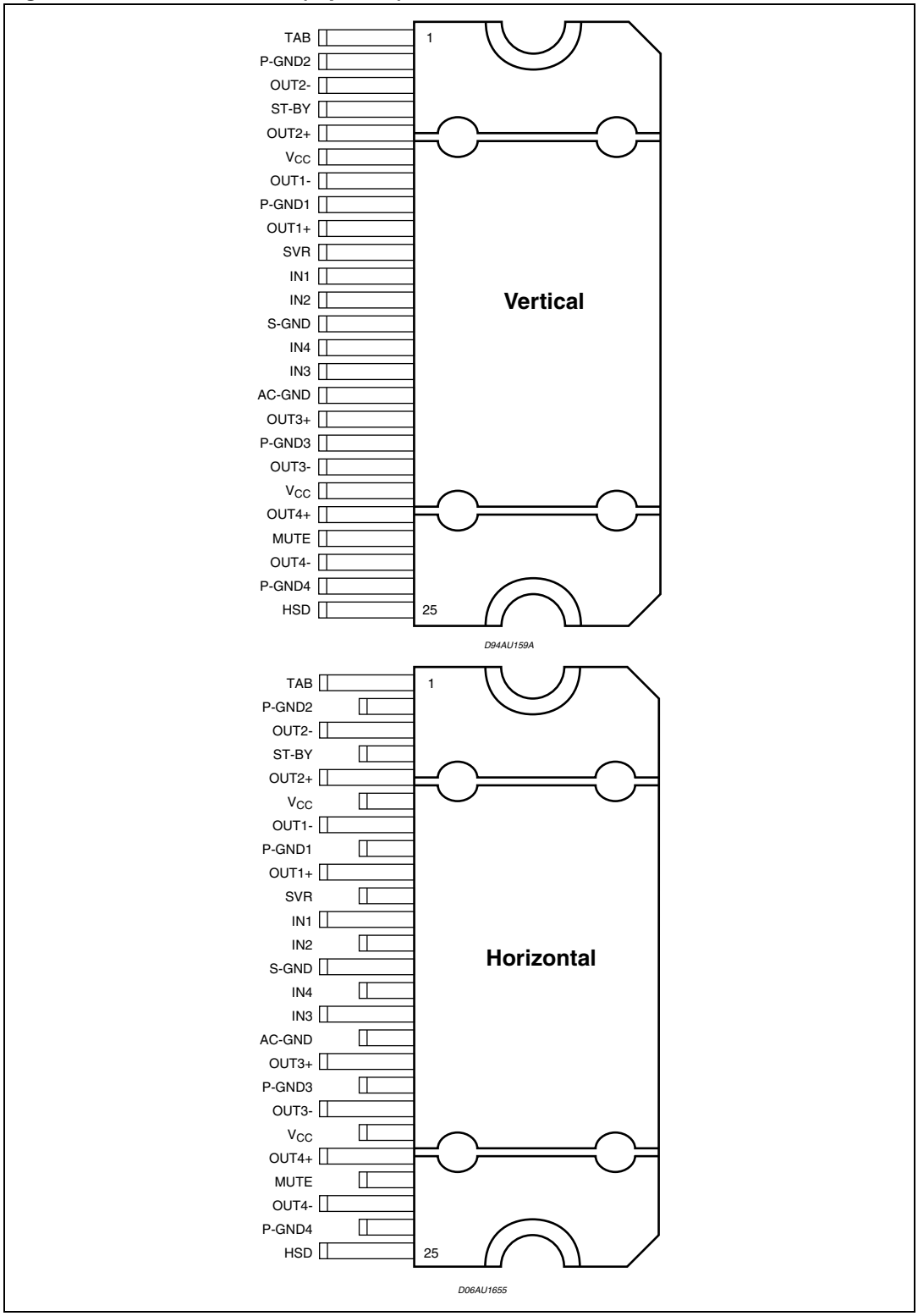
1.2 Standard test and application circuit

Figure 2. Standard test and application circuit



2 Pin description

Figure 3. Pin connection (top view)



3 Electrical specifications

3.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_S	Operating supply voltage	18	V
$V_{S\ (DC)}$	DC supply voltage	28	V
$V_{S\ (pk)}$	Peak supply voltage (for t = 50 ms)	50	V
I_O	Output peak current repetitive (duty cycle 10 % at f = 10 Hz) non repetitive (t = 100 µs)	 9 10	 A A
P_{tot}	Power dissipation T_{case} = 70 °C	80	W
T_j	Junction temperature	150	°C
T_{stg}	Storage temperature	-55 to 150	°C

3.2 Thermal data

Table 3. Thermal data

Symbol	Parameter		Value	Unit
$R_{th\ j\text{-}case}$	Thermal resistance junction to case	Max.	1	°C/W

3.3 Electrical characteristics

Table 4. Electrical characteristics

(Refer to the test and application diagram, V_S = 14.4 V; R_L = 4 Ω; R_g = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified).

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{q1}	Quiescent current	$R_L = \infty$	100	180	280	mA
V_{OS}	Output offset voltage	Play mode / Mute mode			±50	mV
dV_{OS}	During mute ON/OFF output offset voltage	ITU R-ARM weighted see *Figure 20*	-10		+10	mV
	During Standby ON/OFF output offset voltage		-10		+10	mV
G_v	Voltage gain		25	26	27	dB
dG_v	Channel gain unbalance				±1	dB
P_o	Output power	V_S = 13.2 V; THD = 10 % V_S = 13.2 V; THD = 1 % V_S = 14.4 V; THD = 10 % V_S = 14.4 V; THD = 1 %	23 16 28 20	25 19 30 23		W
		V_S = 14.4 V; THD = 10 %, 2 Ω	50	55		W
$P_{o\ max.}$	Max. output power(1)	V_S = 14.4 V; R_L = 4 Ω V_S = 14.4 V; R_L = 2 Ω		50 85		W
THD	Distortion	P_o = 4W P_o = 15W; R_L = 2Ω		0.006 0.015	0.02 0.03	%
e_{No}	Output noise	"A" Weighted Bw = 20 Hz to 20 kHz		35 50	50 70	µV
SVR	Supply voltage rejection	f = 100 Hz; V_r = 1Vrms	50	75		dB
f_{ch}	High cut-off frequency	P_O = 0.5 W	100	300		KHz
R_i	Input impedance		80	100	120	KΩ
C_T	Cross talk	f = 1 kHz P_O = 4 W f = 10 kHz P_O = 4 W	60	70 60	- -	dB
I_{SB}	Standby current consumption	V_{ST-BY} = 1.5 V			20	µA
		V_{ST-BY} = 0 V			10	
I_{pin5}	ST-BY pin current	V_{ST-BY} = 1.5 V to 3.5 V			±1	µA
$V_{SB\ out}$	Standby out threshold voltage	(Amp: ON)	2.75			V
$V_{SB\ in}$	Standby in threshold voltage	(Amp: OFF)			1.5	V
A_M	Mute attenuation	P_{Oref} = 4 W	80	90		dB
$V_{M\ out}$	Mute out threshold voltage	(Amp: Play)	3.5			V
$V_{M\ in}$	Mute in threshold voltage	(Amp: Mute)			1.5	V

Table 4. Electrical characteristics (continued)

(Refer to the test and application diagram, V_S = 14.4 V; R_L = 4 Ω; R_g = 600 Ω; f = 1 kHz; T_{amb} = 25 °C; unless otherwise specified).

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
$V_{AM\ in}$	V_S automute threshold	(Amp: Mute) Att ≥ 80 dB; P_{Oref} = 4 W (Amp: Play) Att < 0.1 dB; P_O = 0. 5W	6.5	7 7.5	 8	V
I_{pin23}	Muting pin current	V_{MUTE} = 1.5 V (Sourced Current)	7	12	18	µA
		V_{MUTE} = 3.5 V	-5		18	µA
HSD section						
$V_{dropout}$	Dropout voltage	I_O = 0.35 A; V_S = 9 to 16 V		0.25	0.6	V
I_{prot}	Current limits		400		800	mA
Offset detector (Pin 25)						
V_{M_ON}	Mute voltage for DC offset detection enabled	V_{ST-BY} = 5 V	8			V
V_{M_OFF}					6	V
V_{OFF}	Detected differential output offset	V_{ST-BY} = 5 V; V_{mute} = 8 V	±2	±3	±4	V
V_{25_T}	Pin 25 voltage for detection = TRUE	V_{ST-BY} = 5 V; V_{mute} = 8 V V_{OFF} > ±4 V	0		1.5	V
V_{25_F}	Pin 25 Voltage for detection = FALSE	V_{ST-BY} = 5 V; V_{mute} = 8 V V_{OFF} > ±2 V	12			V

1. Saturated square wave output.

Figure 4. Components and top copper layer of the *Figure 2*.

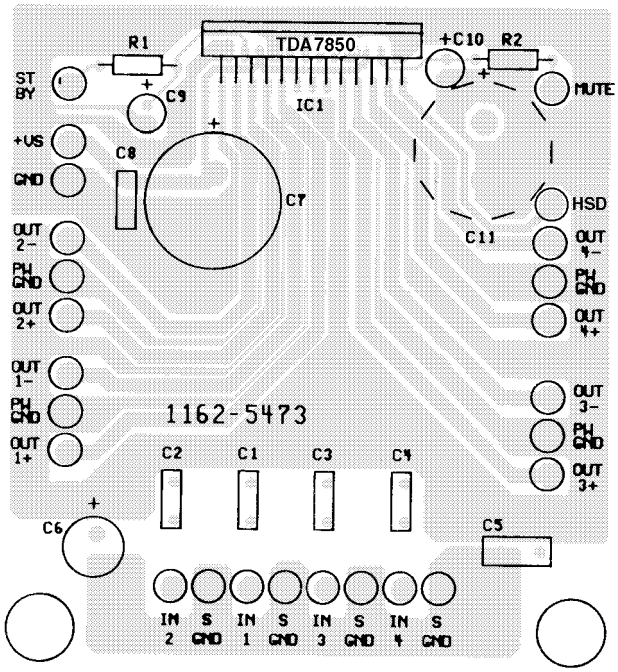
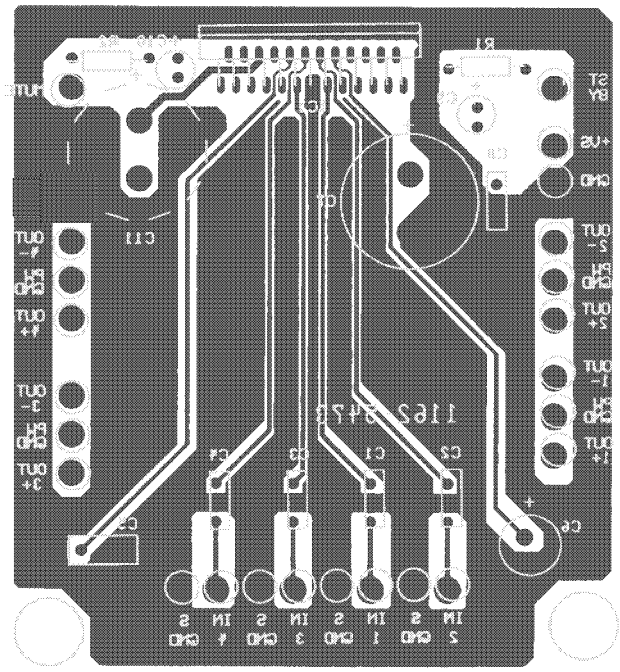


Figure 5. Bottom copper layer *Figure 2*.



3.4 Electrical characteristic curves

Figure 6. Quiescent current vs. supply voltage

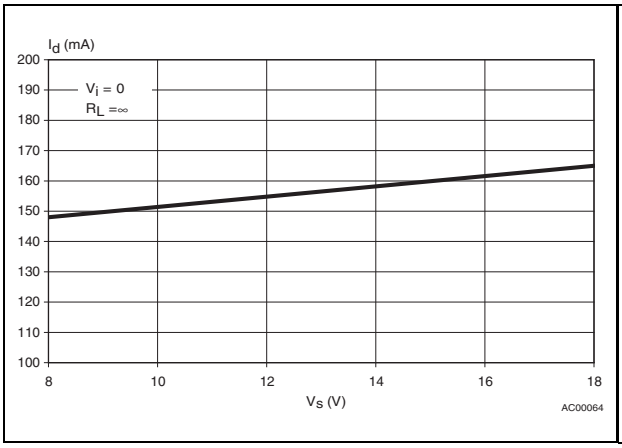


Figure 7. Output power vs. supply voltage (R_L = 4Ω)

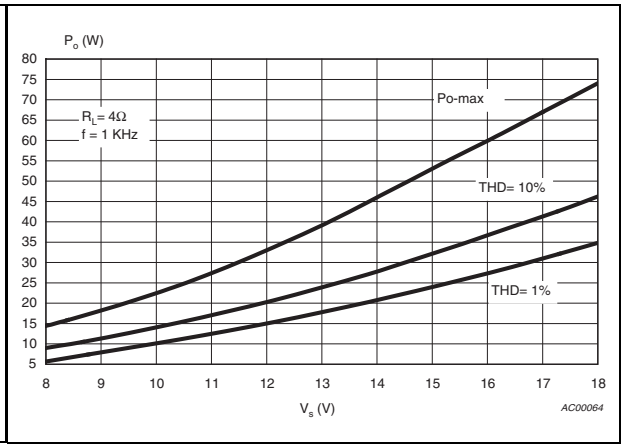


Figure 8. Output power vs. supply voltage (R_L = 2Ω)

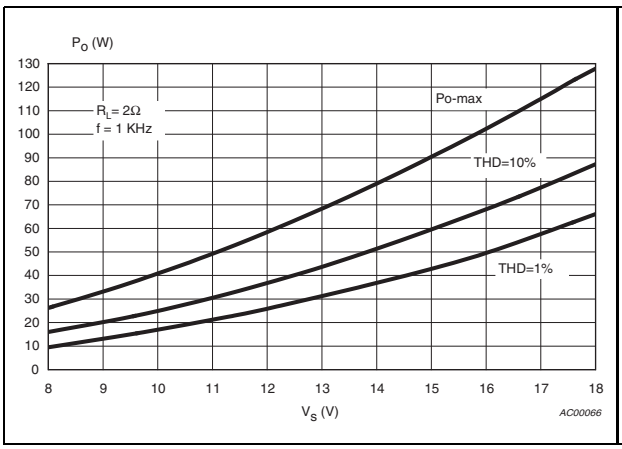


Figure 9. Distortion vs. output power (R_L = 4Ω)

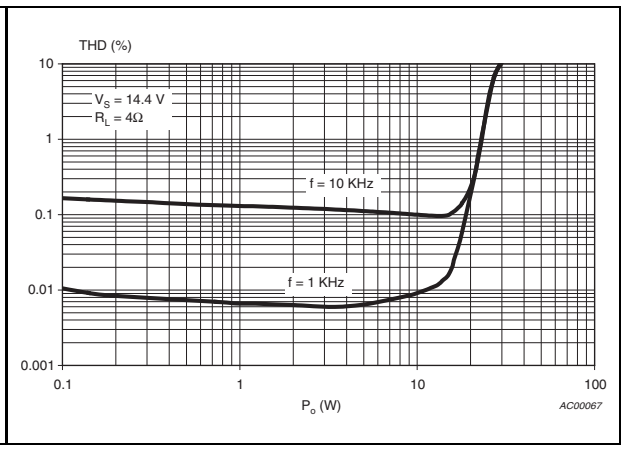


Figure 10. Distortion vs. output power (R_L = 2Ω)

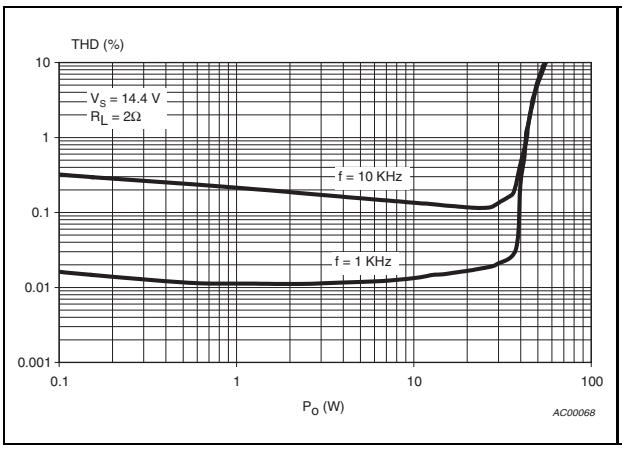


Figure 11. Distortion vs. frequency (R_L = 4Ω)

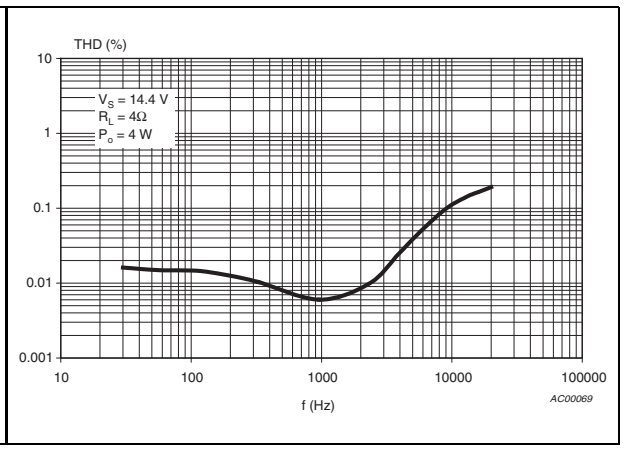


Figure 12. Distortion vs. frequency (R_L = 2Ω)

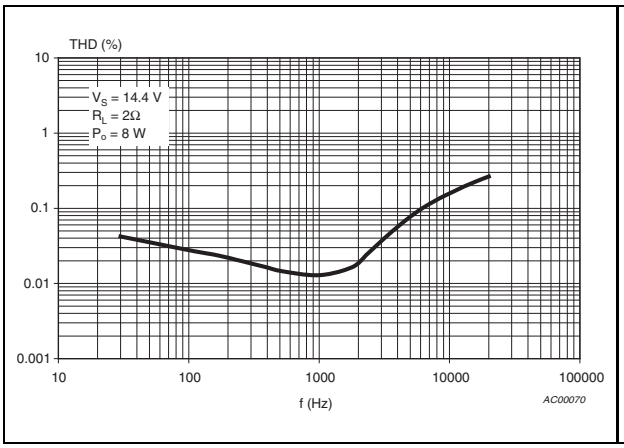


Figure 13. Crosstalk vs. frequency

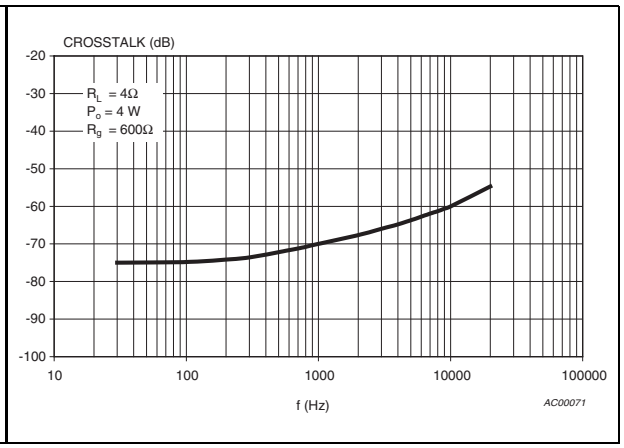


Figure 14. Supply voltage rejection vs. frequency

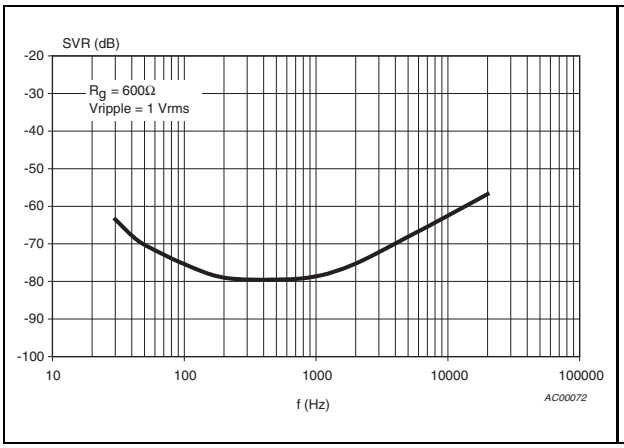


Figure 15. Output attenuation vs. supply voltage

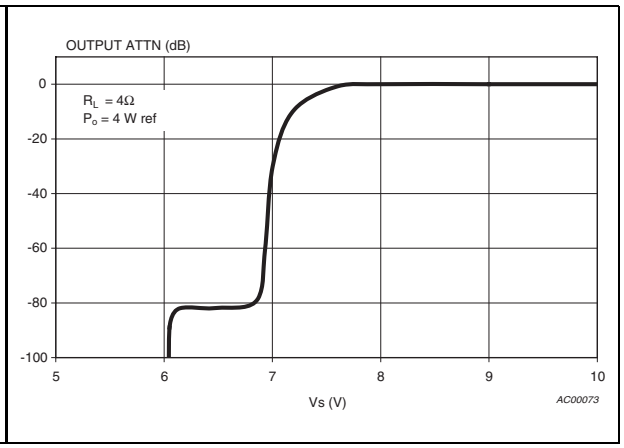


Figure 16. Power dissipation and efficiency vs. output power (R_L = 4Ω, SINE)

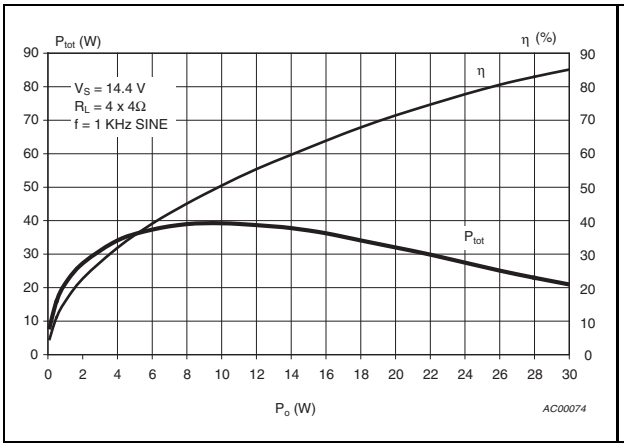


Figure 17. Power dissipation and efficiency vs. output power (R_L = 2Ω, SINE)

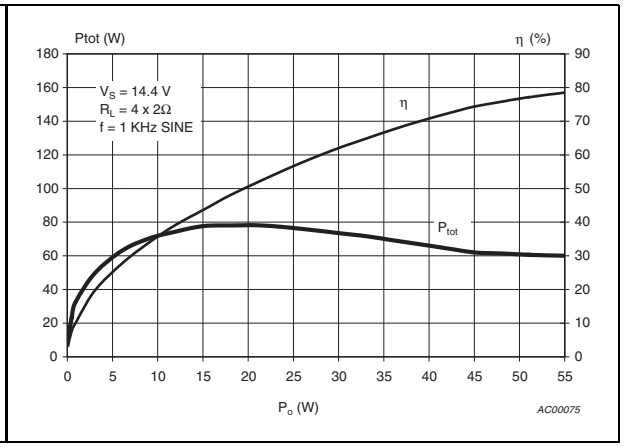


Figure 18. Power dissipation vs. output power (R_L = 4Ω, audio program simulation)

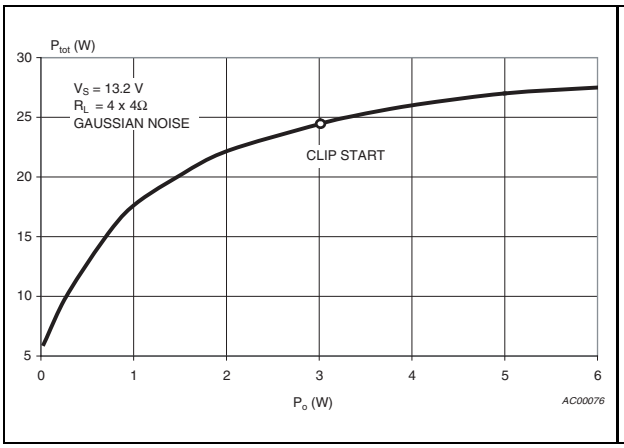


Figure 19. Power dissipation vs. output power (R_L = 2Ω, audio program simulation)

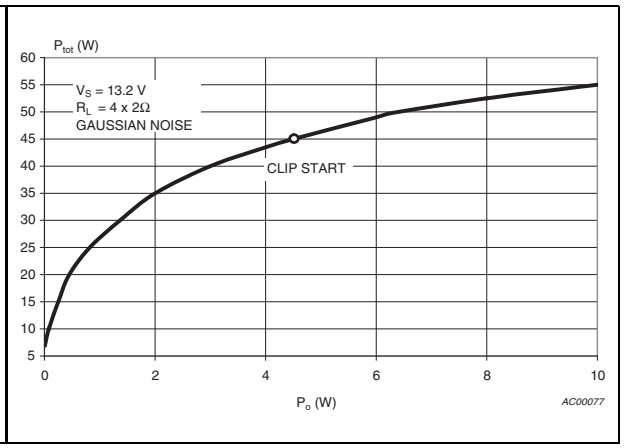
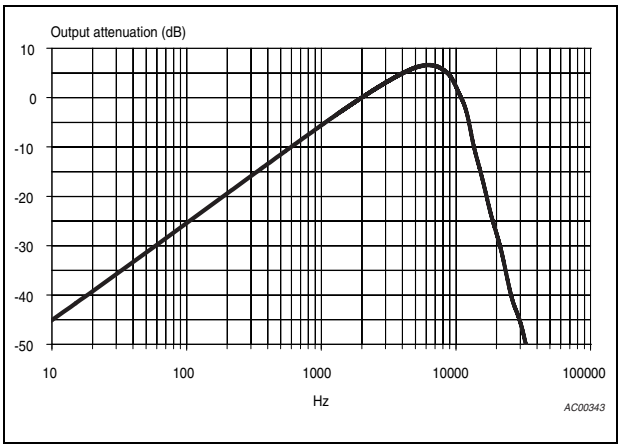


Figure 20. ITU R-ARM frequency response, weighting filter for transient pop



4 Application hints

Referred to the circuit of *Figure 2*.

4.1 SVR

Besides its contribution to the ripple rejection, the SVR capacitor governs the turn ON/OFF time sequence and, consequently, plays an essential role in the pop optimization during ON/OFF transients. To conveniently serve both needs, **Its minimum recommended value is 10µF**.

4.2 Input stage

The TDA7850's inputs are ground-compatible and can stand very high input signals (± 8Vpk) without any performance degradation.
If the standard value for the input capacitors (0.1µF) is adopted, the low frequency cut-off will amount to 16 Hz.

4.3 Standby and muting

Standby and Muting facilities are both CMOS compatible. In absence of true CMOS ports or microprocessors, a direct connection to Vs of these two pins is admissible but a 470kΩ equivalent resistance should be present between the power supply and the muting and ST-BY pins.
R-C cells have always to be used in order to smooth down the transitions for preventing any audible transient noises.
About the standby, the time constant to be assigned in order to obtain a virtually pop-free transition has to be slower than 2.5 V/ms.

4.4 DC offset detector

The TDA7850 integrates a DC offset detector to avoid that an anomalous DC offset on the inputs of the amplifier may be multiplied by the gain and result in a dangerous large offset on the outputs which may lead to speakers damage for overheating. The feature is enabled by the MUTE pin (according to table 3) and works with the amplifier unmuted and with no signal on the inputs.
The DC offset detection is signaled out on the HSD pin. To ensure the correct functionality of the Offset Detector it is necessary to connect a pulldown 10 kW resistor between HSD and ground.

4.5 Heatsink definition

Under normal usage (4 Ohm speakers) the heatsink's thermal requirements have to be deduced from *Figure 18*, which reports the simulated power dissipation when real music/speech programmes are played out. Noise with gaussian-distributed amplitude was employed for this simulation. Based on that, frequent clipping occurrence (worst-case) will cause P_{diss} = 26 W. Assuming T_{amb} = 70 °C and T_{CHIP} = 150 °C as boundary conditions, the heatsink's thermal resistance should be approximately 2°C/W. This would avoid any thermal shutdown occurrence even after long-term and full-volume operation.

5 Package information

In order to meet environmental requirements, ST (also) offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

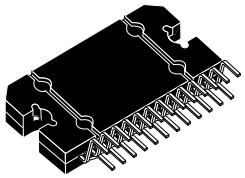
ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 21. Flexiwatt25 (vertical) mechanical data and package dimensions

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D	0.75	0.90	1.05	0.029	0.035	0.041
E	0.37	0.39	0.42	0.014	0.015	0.016
F (1)			0.57			0.022
G	0.80	1.00	1.20	0.031	0.040	0.047
G1	23.75	24.00	24.25	0.935	0.945	0.955
H (2)	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L (2)	22.07	22.47	22.87	0.869	0.884	0.904
L1	18.57	18.97	19.37	0.731	0.747	0.762
L2 (2)	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5		3.5			0.138	
M	3.70	4.00	4.30	0.145	0.157	0.169
M1	3.60	4.00	4.40	0.142	0.157	0.173
N		2.20			0.086	
O		2			0.079	
R		1.70			0.067	
R1		0.5			0.02	
R2		0.3			0.12	
R3		1.25			0.049	
R4		0.50			0.019	
V	5° (T p.)					
V1	3° (Typ.)					
V2	20° (Typ.)					
V3	45° (Typ.)					

(1): dam-bar protusion not included
(2): molding protusion included

OUTLINE AND MECHANICAL DATA



Flexiwatt25 (vertical)

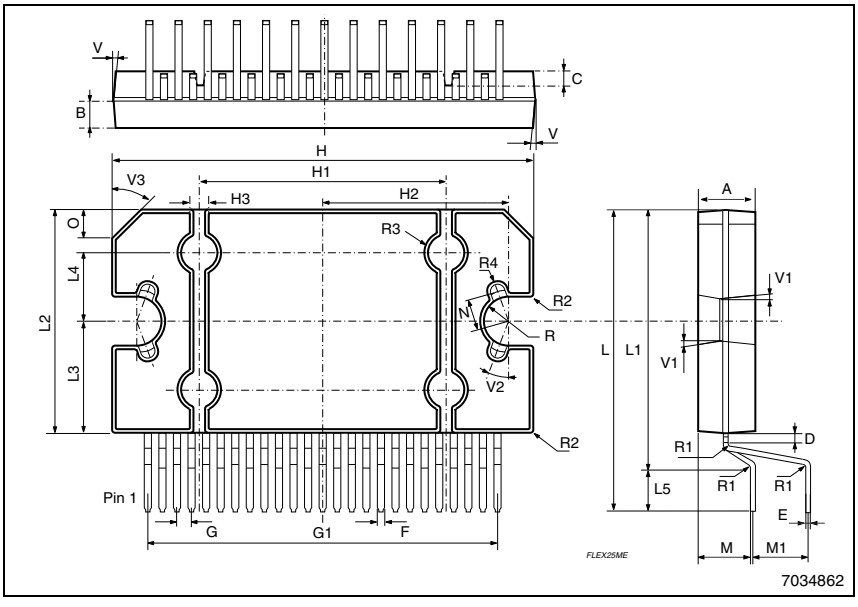
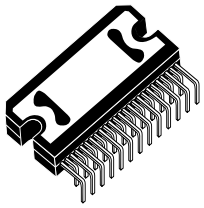


Figure 22. Flexiwatt25 (horizontal) mechanical data and package dimensions

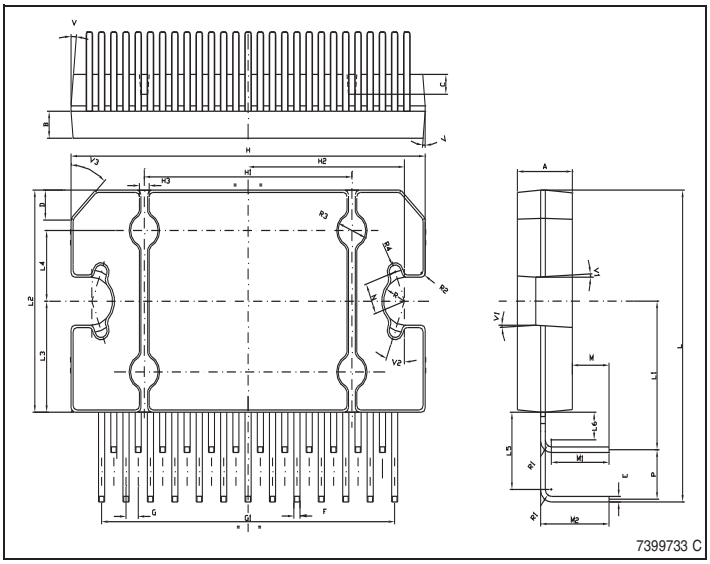
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.45	4.50	4.65	0.175	0.177	0.183
B	1.80	1.90	2.00	0.070	0.074	0.079
C		1.40			0.055	
D		2.00			0.079	
E	0.37	0.39	0.42	0.014	0.015	0.016
F (1)			0.57			0.022
G	0.75	1.00	1.25	0.029	0.040	0.049
G1	23.70	24.00	24.30	0.933	0.945	0.957
H (2)	28.90	29.23	29.30	1.139	1.150	1.153
H1		17.00			0.669	
H2		12.80			0.503	
H3		0.80			0.031	
L (2)	21.64	22.04	22.44	0.852	0.868	0.883
L1	10.15	10.5	10.85	0.40	0.413	0.427
L2 (2)	15.50	15.70	15.90	0.610	0.618	0.626
L3	7.70	7.85	7.95	0.303	0.309	0.313
L4		5			0.197	
L5	5.15	5.45	5.85	0.203	0.214	0.23
L6	1.80	1.95	2.10	0.070	0.077	0.083
M	2.75	3.00	3.50	0.108	0.118	0.138
M1		4.73			0.186	
M2		5.61			0.220	
N		2.20			0.086	
P	3.20	3.50	3.80	0.126	0.138	0.15
R		1.70			0.067	
R1		0.50			0.02	
R2		0.30			0.12	
R3		1.25			0.049	
R4		0.50			0.02	
V	5° (Typ.)					
V1	3° (Typ.)					
V2	20° (Typ.)					
V3	45° (Typ.)					

(1): dam-bar protusion not included; (2): molding protusion included

OUTLINE AND MECHANICAL DATA



Flexiwatt25 (Horizontal)



6 Revision history

Table 5. Document revision history

Date	Revision	Changes
22-Nov-2006	1	Initial release.
27-Feb-2007	2	Added *Chapter 3.4: Electrical characteristic curves*.
09-Oct-2007	3	Updated the values for the dV_{OS} and I_{q1} parameters on the *Table 4*. Added *Figure 20 on page 13*.
12-Sep-2008	4	Updated *Figure 2: Standard test and application circuit*. Updated *Section 4.4: DC offset detector* and *Section 4.3: Standby and muting*. Updated the values of V_{OS} and THD parameters on the *Table 4*.
07-Nov-2008	5	Modified max. values of the THD distortion in *Table 4: Electrical characteristics on page 8*.
17-Sep-2013	6	Updated Disclaimer.

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