

ST(意法) STW75NF20 **PDF**

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STB75NF20 STP75NF20 - STW75NF20

N-channel 200V - 0.028Ω - 75A - D²PAK - TO-220 - TO-247
Low gate charge STripFET™ Power MOSFET

General features

Type	V _{DSS}	R _{DS(on)}	I _D
STB75NF20	200V	<0.034Ω	75A
STP75NF20	200V	<0.034Ω	75A
STW75NF20	200V	<0.034Ω	75A

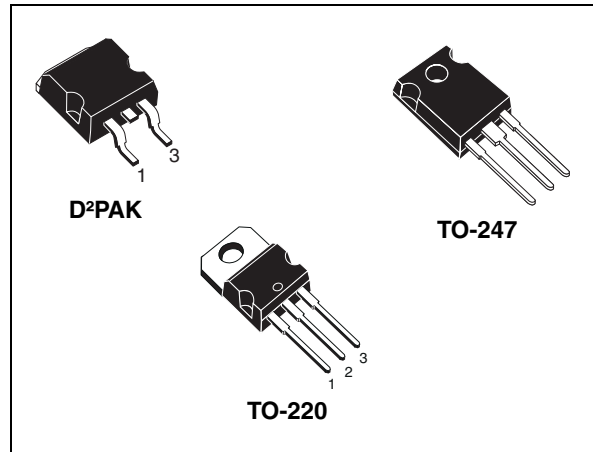
- Exceptional dv/dt capability
- Low gate charge
- 100% Avalanche tested

Description

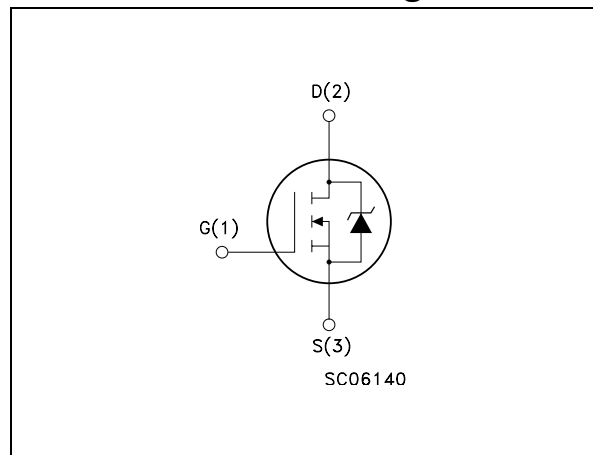
This Power MOSFET series realized with STMicroelectronics unique STripFET™ process has specifically been designed to minimize input capacitance and gate charge. It is therefore suitable as primary switch in advanced high-efficiency isolated DC-DC converters

Applications

- Switching application



Internal schematic diagram



Order codes

Part number	Marking	Package	Packaging
STB75NF20	75NF20	D ² PAK	Tape & reel
STP75NF20	75NF20	TO-220	Tube
STW75NF20	75NF20	TO-247	Tube

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1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage ($V_{GS} = 0$)	200	V
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current (continuous) at $T_C = 25^\circ\text{C}$	75	A
I_D	Drain current (continuous) at $T_C = 100^\circ\text{C}$	47	A
$I_{DM}^{(1)}$	Drain current (pulsed)	300	A
	Derating factor	1.52	W/ $^\circ\text{C}$
dv/dt	Peak diode recovery voltage slope	15	V/ns
P_{TOT}	Total dissipation at $T_C = 25^\circ\text{C}$	190	W
T_J T_{stg}	Operating junction temperature Storage temperature	-50 to 150	$^\circ\text{C}$

1. $I_{SD} \leq 75\text{A}$, $di/dt \leq 400\text{A}/\mu\text{s}$, $V_{DD} \leq 160$

Table 2. Thermal resistance

Symbol	Parameter	Value		Unit
		TO-220/D ² PAK	TO-247	
R_{thJC}	Thermal resistance junction-case max	0.66		$^\circ\text{C}/\text{W}$
$R_{thJ-pcb}^{(1)}$	Thermal resistance junction-pcb max	34	--	$^\circ\text{C}/\text{W}$
R_{thJA}	Thermal resistance junction-ambient max	62.5	40	$^\circ\text{C}/\text{W}$
T_l	Maximum lead temperature for soldering purpose	300		$^\circ\text{C}$

1. When mounted on inch²FR-4 board ($t \leq 10\mu\text{s}$)

Table 3. Avalanche characteristics

Symbol	Parameter	Max value	Unit
I_{AR}	Avalanche current, repetitive or not-repetitive (pulse width limited by T_J max)	37	A
E_{AS}	Single pulse avalanche energy (starting $T_J = 25^\circ\text{C}$, $I_d = I_{AR}$, $V_{dd} = 50\text{V}$)	205	mJ

2 Electrical characteristics

($T_{CASE}=25^{\circ}\text{C}$ unless otherwise specified)

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{mA}$, $V_{GS} = 0$	200			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = \text{Max rating}$, $V_{DS} = \text{Max rating @ } 125^{\circ}\text{C}$			1 10	μA μA
I_{GSS}	Gate body leakage current ($V_{DS} = 0$)	$V_{DS} = \pm 20\text{V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{V}$, $I_D = 37\text{A}$		0.028	0.034	Ω

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 15\text{V}$, $I_D = 37\text{A}$		40		S
C_{iss}	Input capacitance	$V_{DS} = 25\text{V}$, $f = 1\text{MHz}$, $V_{GS} = 0$		3260		pF
C_{oss}	Output capacitance			640		pF
C_{rss}	Reverse Transfer Capacitance			110		pF
Q_g	Total gate charge	$V_{DD} = 160\text{V}$, $I_D = 75\text{A}$,		84		nC
Q_{gs}	Gate-source charge	$V_{GS} = 10\text{V}$		18		nC
Q_{gd}	Gate-drain charge	(see Figure 16)		34		nC

1. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 100\text{V}$, $I_D = 37\text{A}$ $R_G = 4.7\Omega$, $V_{GS} = 10\text{V}$, (see Figure 15)		53		ns
t_r	Rise time			33		ns
$t_{d(off)}$	Turn-off delay time			75		ns
t_f	Fall time			29		ns

Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current				75	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				300	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 75A, V_{GS} = 0$			1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 75A, V_{DD} = 100V$ $di/dt = 100 A/\mu s$ $T_j = 25^\circ C$ (see Figure 20)		222		ns
Q_{rr}	Reverse recovery charge			2.18		μC
I_{RRM}	Reverse recovery current			19		A
t_{rr}	Reverse recovery time	$I_{SD} = 75A, V_{DD} = 100V$ $di/dt = 100 A/\mu s$ $T_j = 150^\circ C$ (see Figure 20)		267		ns
Q_{rr}	Reverse recovery charge			3		μC
I_{RRM}	Reverse recovery current			22		A

1. Pulse with limited by maximum temperature

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area for TO-220 / D²PAK

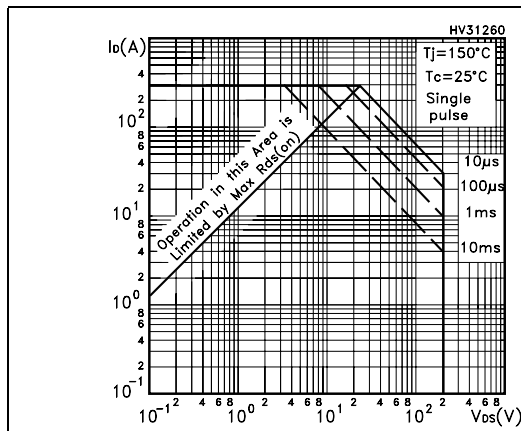


Figure 2. Thermal impedance for TO-220 / D²PAK

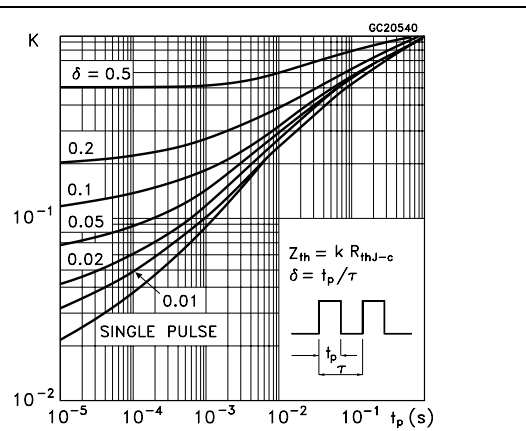


Figure 3. Safe operating area for TO-247

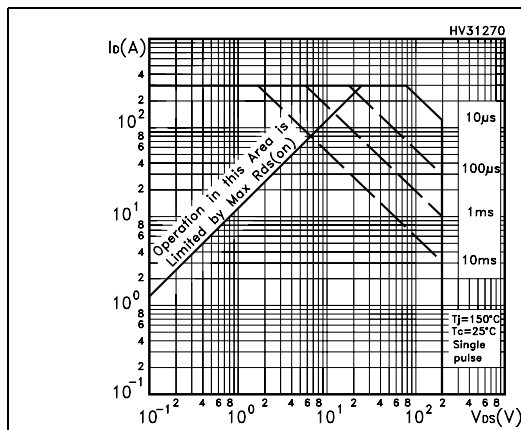


Figure 4. Thermal impedance for TO-247

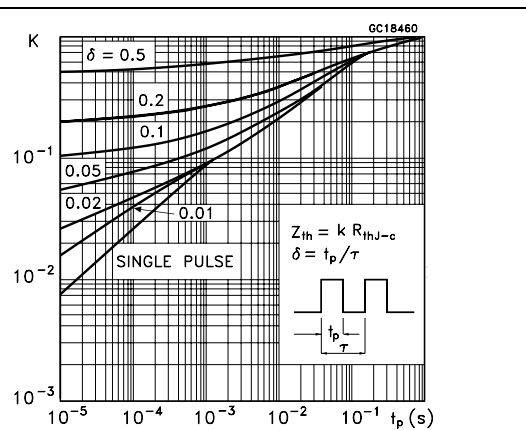


Figure 5. Output characteristics

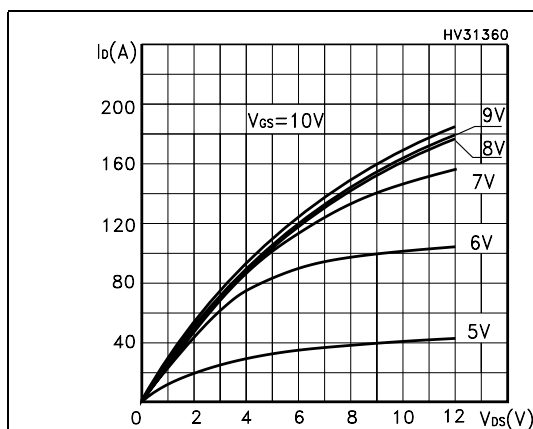


Figure 6. Transfer characteristics

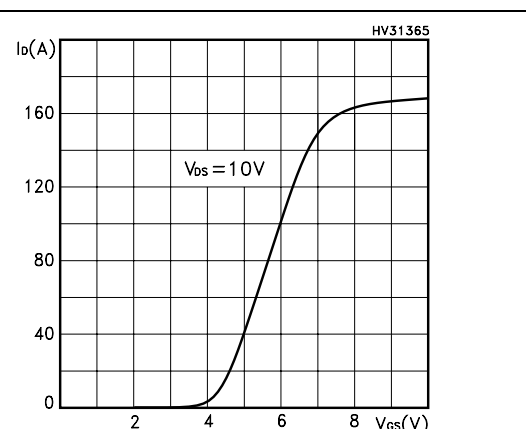


Figure 7. Normalized $B_{V_{DS}}$ vs temperature Figure 8. Static drain-source on resistance

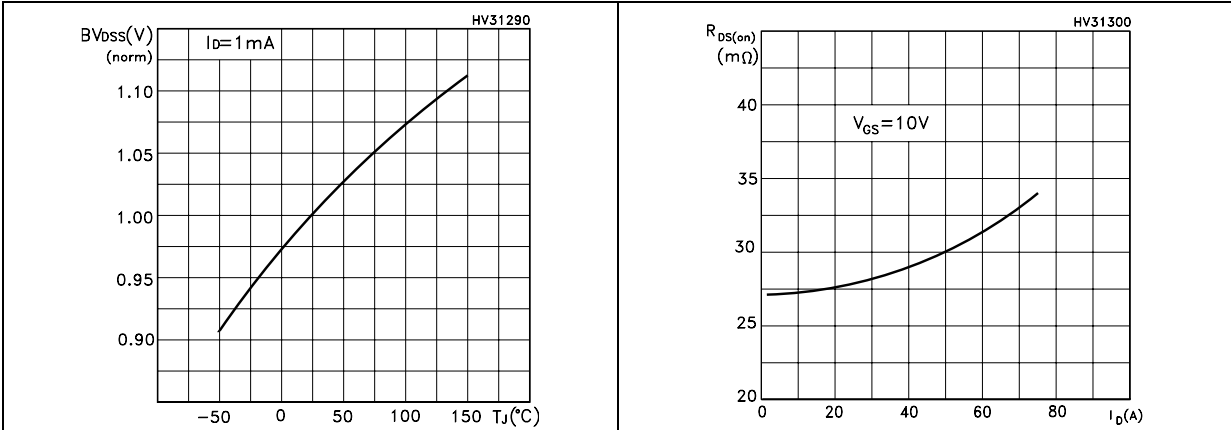


Figure 9. Gate charge vs gate-source voltage Figure 10. Capacitance variations

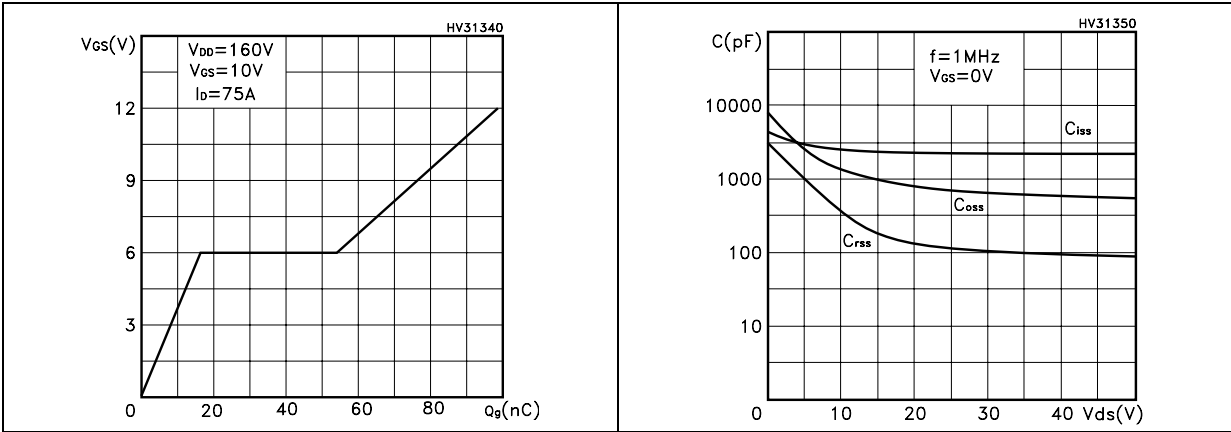


Figure 11. Normalized gate threshold voltage vs temperature Figure 12. Normalized on resistance vs temperature

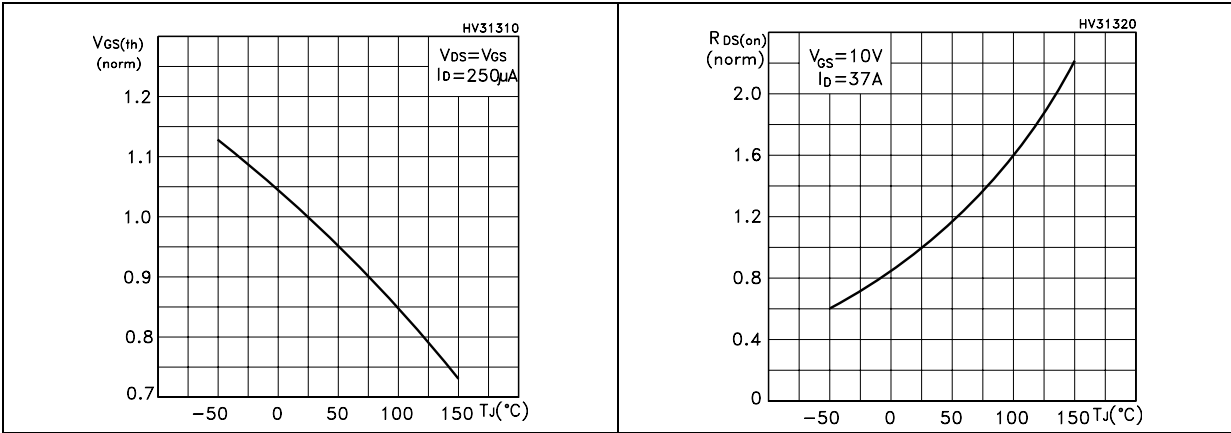


Figure 13. Source-drain diode forward characteristics

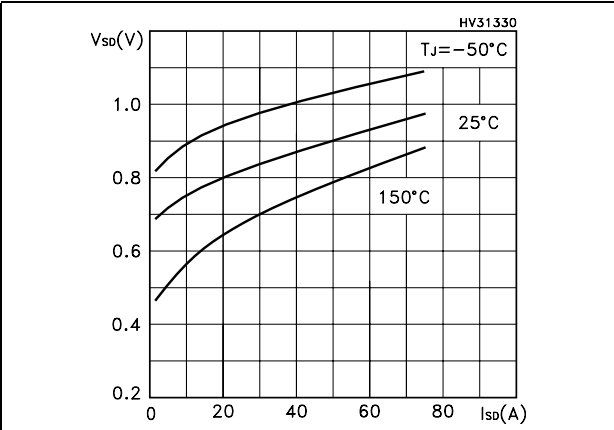
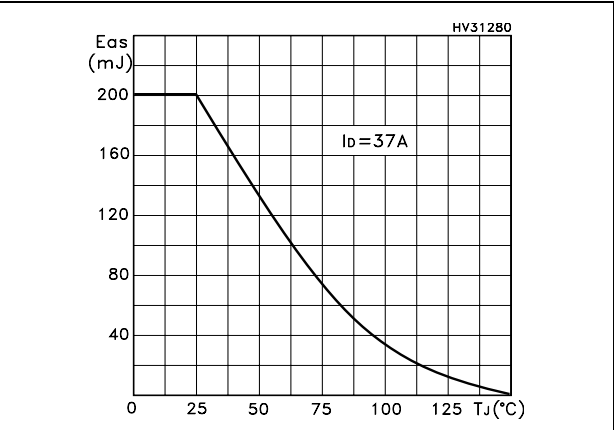


Figure 14. Avalanche energy vs starting T_J



3 Test circuit

Figure 15. Switching times test circuit for resistive load

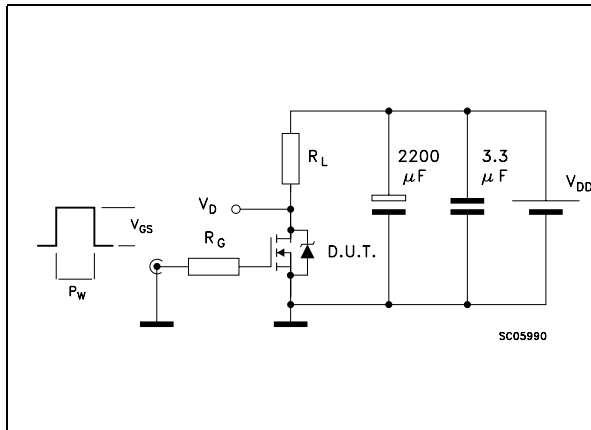


Figure 16. Gate charge test circuit

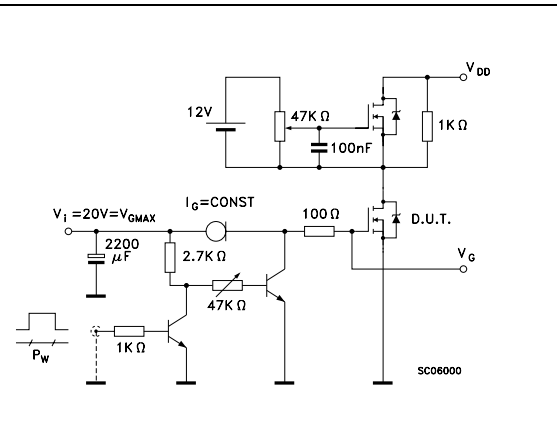


Figure 17. Test circuit for inductive load switching and diode recovery times

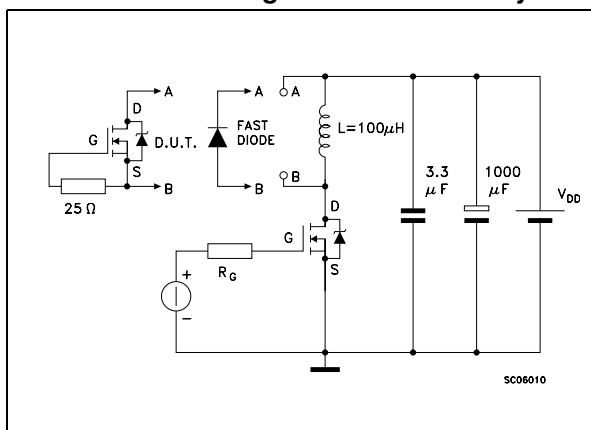


Figure 18. Unclamped inductive load test circuit

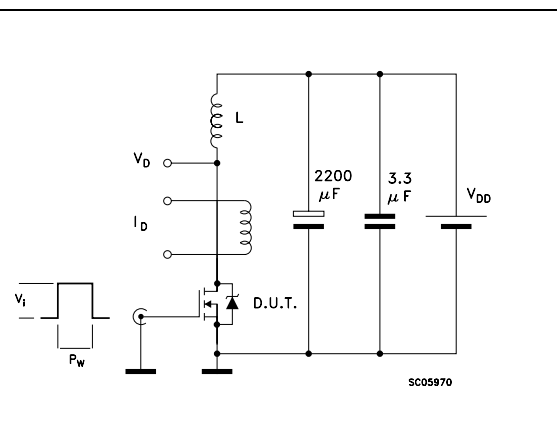


Figure 19. Unclamped inductive waveform

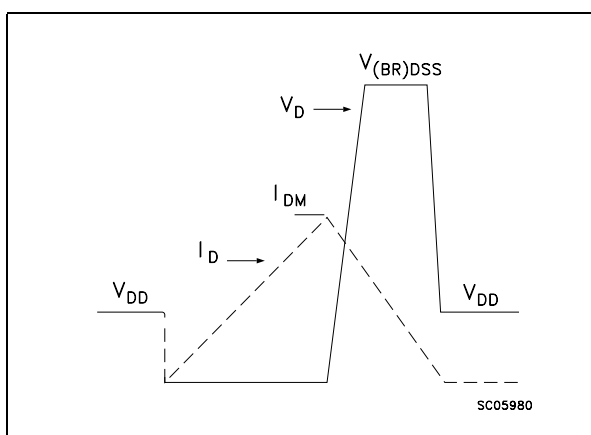
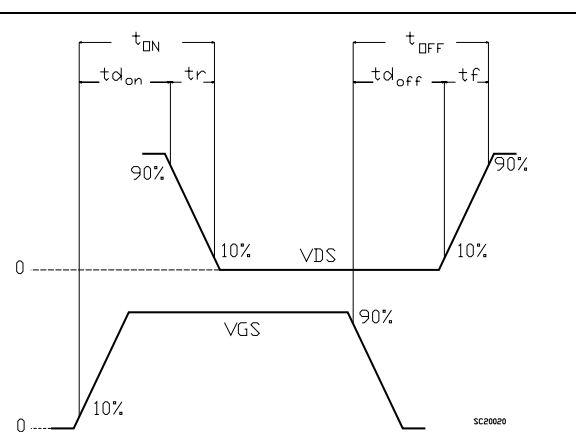


Figure 20. Switching time waveform

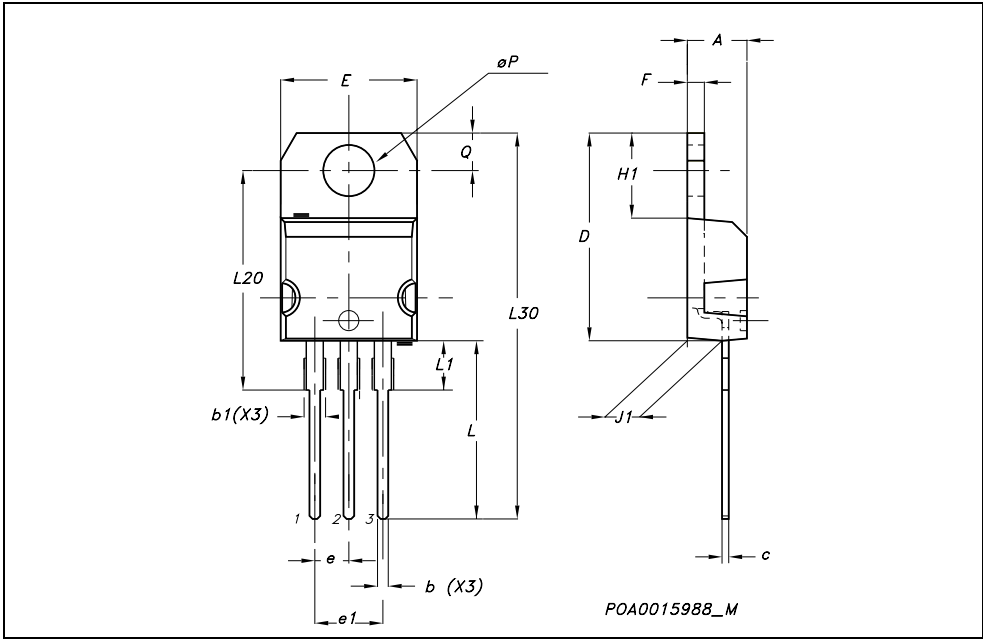


4 **Package mechanical data**

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at : www.st.com

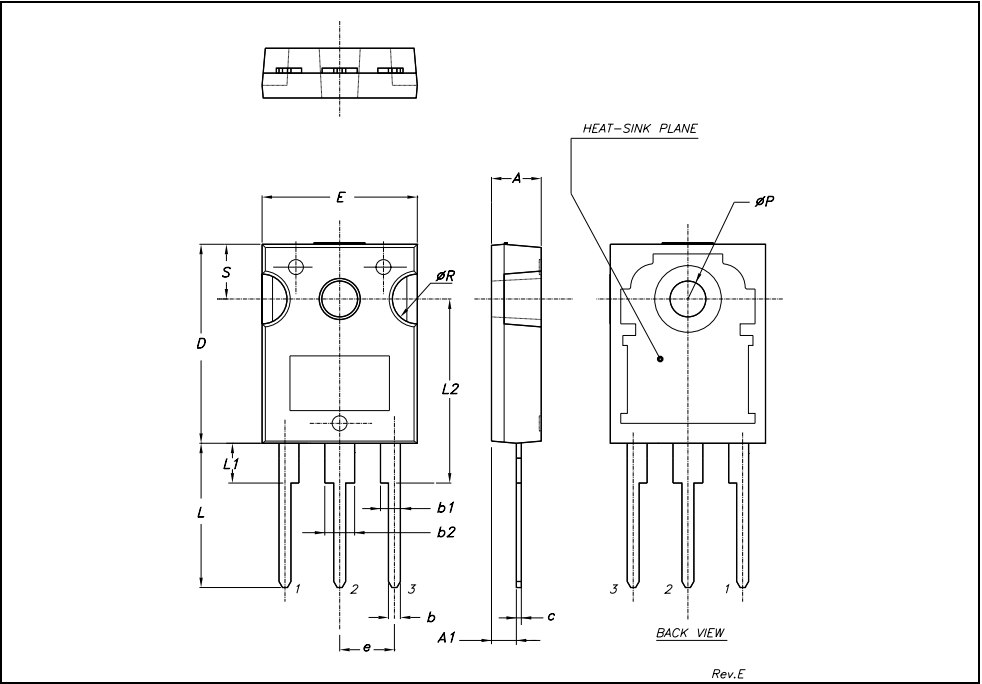
TO-220 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
b	0.61		0.88	0.024		0.034
b1	1.15		1.70	0.045		0.066
c	0.49		0.70	0.019		0.027
D	15.25		15.75	0.60		0.620
E	10		10.40	0.393		0.409
e	2.40		2.70	0.094		0.106
e1	4.95		5.15	0.194		0.202
F	1.23		1.32	0.048		0.052
H1	6.20		6.60	0.244		0.256
J1	2.40		2.72	0.094		0.107
L	13		14	0.511		0.551
L1	3.50		3.93	0.137		0.154
L20		16.40			0.645	
L30		28.90			1.137	
øP	3.75		3.85	0.147		0.151
Q	2.65		2.95	0.104		0.116



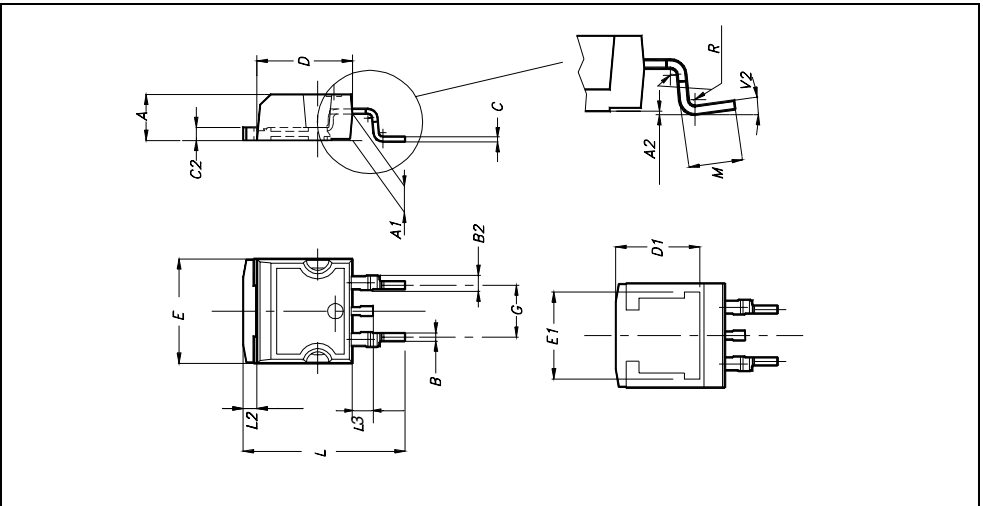
TO-247 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.85		5.15	0.19		0.20
A1	2.20		2.60	0.086		0.102
b	1.0		1.40	0.039		0.055
b1	2.0		2.40	0.079		0.094
b2	3.0		3.40	0.118		0.134
c	0.40		0.80	0.015		0.03
D	19.85		20.15	0.781		0.793
E	15.45		15.75	0.608		0.620
e		5.45			0.214	
L	14.20		14.80	0.560		0.582
L1	3.70		4.30	0.14		0.17
L2		18.50			0.728	
øP	3.55		3.65	0.140		0.143
øR	4.50		5.50	0.177		0.216
S		5.50			0.216	



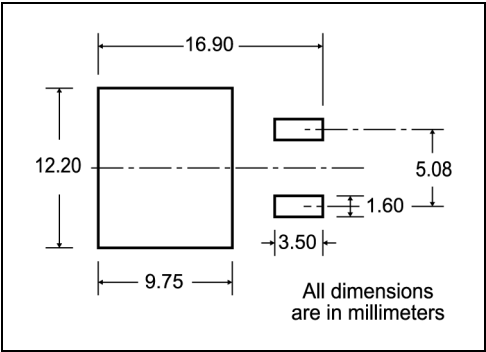
D²PAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
A1	2.49		2.69	0.098		0.106
A2	0.03		0.23	0.001		0.009
B	0.7		0.93	0.027		0.036
B2	1.14		1.7	0.044		0.067
C	0.45		0.6	0.017		0.023
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
D1		8			0.315	
E	10		10.4	0.393		
E1		8.5			0.334	
G	4.88		5.28	0.192		0.208
L	15		15.85	0.590		0.625
L2	1.27		1.4	0.050		0.055
L3	1.4		1.75	0.055		0.068
M	2.4		3.2	0.094		0.126
R		0.4			0.015	
V2	0°		4°			

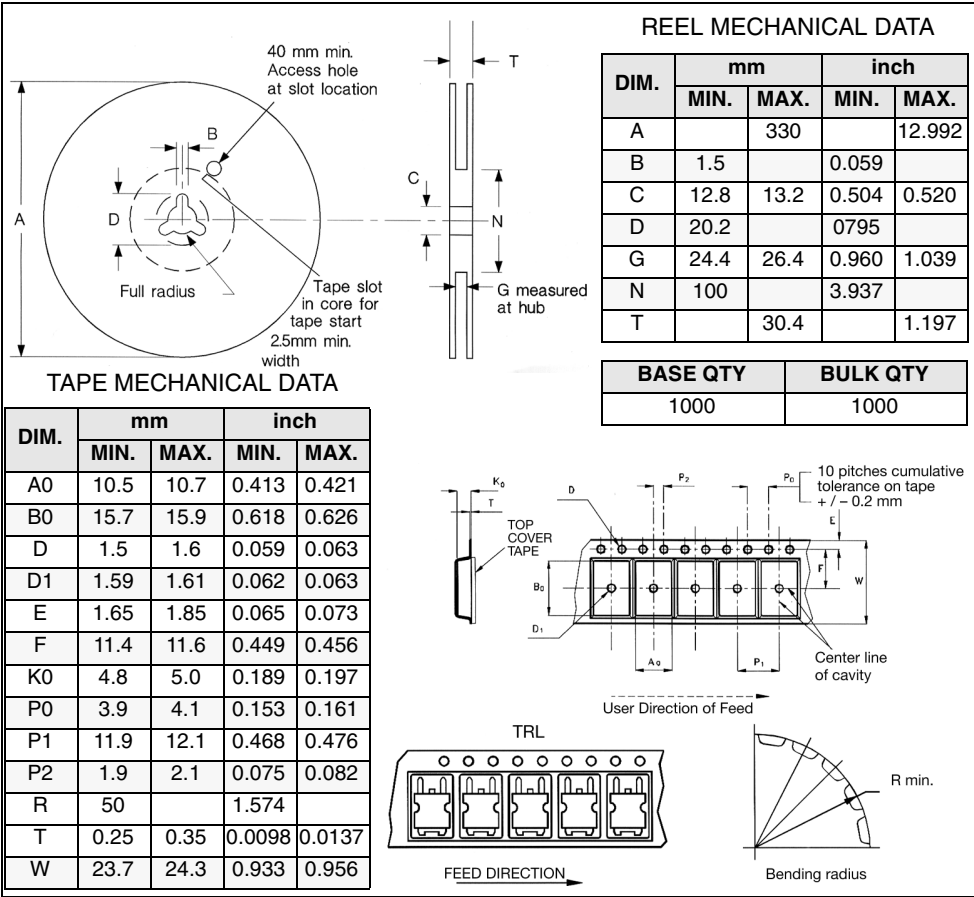


5 Packaging mechanical data

D²PAK FOOTPRINT



TAPE AND REEL SHIPMENT



* on sales type

6 Revision history

Table 8. Revision history

Date	Revision	Changes
30-Jan-2007	1	First release
21-Mar-2007	2	Complete version

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