ST(意法) L3GD20 PDF

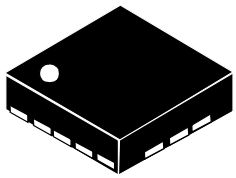
深圳创唯电子有限公司

http://www.st-ic.com

L3GD20H

MEMS motion sensor: three-axis digital output gyroscope

Datasheet - production data



LGA-16 (3x3x1 mm)

Features

- Wide supply voltage, 2.2 V to 3.6 V
- Wide extended operating temperature range (from -40 °C to 85 °C)
- Low voltage compatible IOs, 1.8 V
- Low power consumption
- Embedded power-down
- Sleep mode
- Fast turn-on and wake-up
- Three selectable full scales up to 2000 dps
- 16 bit rate value data output
- 8 bit temperature data output
- I^2C/SPI digital output interface
- 2 dedicated lines (1 interrupt, 1 data ready)
- User enable integrated high-pass filters
- Embedded temperature sensor
- Embedded 32 levels of 16 bit data output FIFO
- High shock survivability
- ECOPACK® RoHS and “Green” compliant

Applications

- Gaming and virtual reality input devices
- Motion control with MMI (man-machine interface)
- GPS navigation systems
- Appliances and robotics

Description

The L3GD20H is a low-power three-axis angular rate sensor.

It includes a sensing element and an IC interface able to provide the measured angular rate to the external world through digital interface (I^2C/SPI).

The sensing element is manufactured using a dedicated micromachining process developed by ST to produce inertial sensors and actuators on silicon wafers.

The IC interface is manufactured using a CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the sensing element characteristics.

The L3GD20H has a full scale of ±245/±500/±2000 dps and is capable of measuring rates with a user selectable bandwidth.

The L3GD20H is available in a plastic land grid array (LGA) package and can operate within a temperature range from -40 °C to +85 °C.

Table 1. Device summary

Order code	Temperature range (°C)	Package	Packing
L3GD20H	-40 to +85	LGA-16 (3x3x1)	Tray
L3GD20HTR	-40 to +85	LGA-16 (3x3x1)	Tape and reel

This is information on a product in full production. www.st.com

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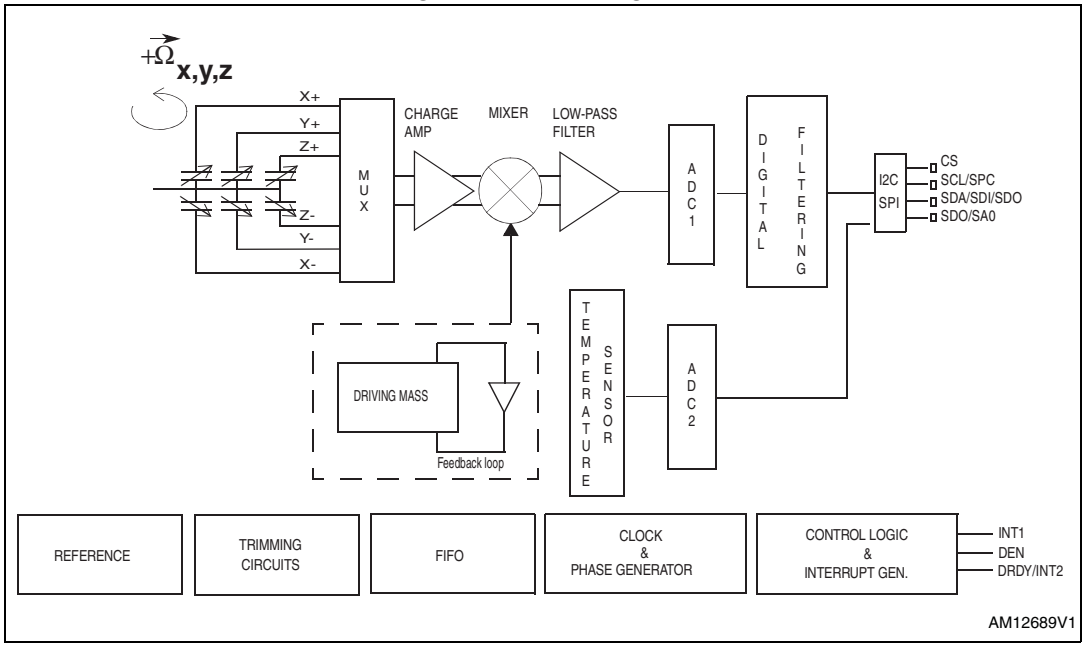
1 Block diagram and pin description

Figure 1. Block diagram



The vibration of the structure is maintained by a drive circuitry in a feedback loop. The sensing signal is filtered and appears as digital signal at the output.

1.1 Pin description

Figure 2. Pin connection

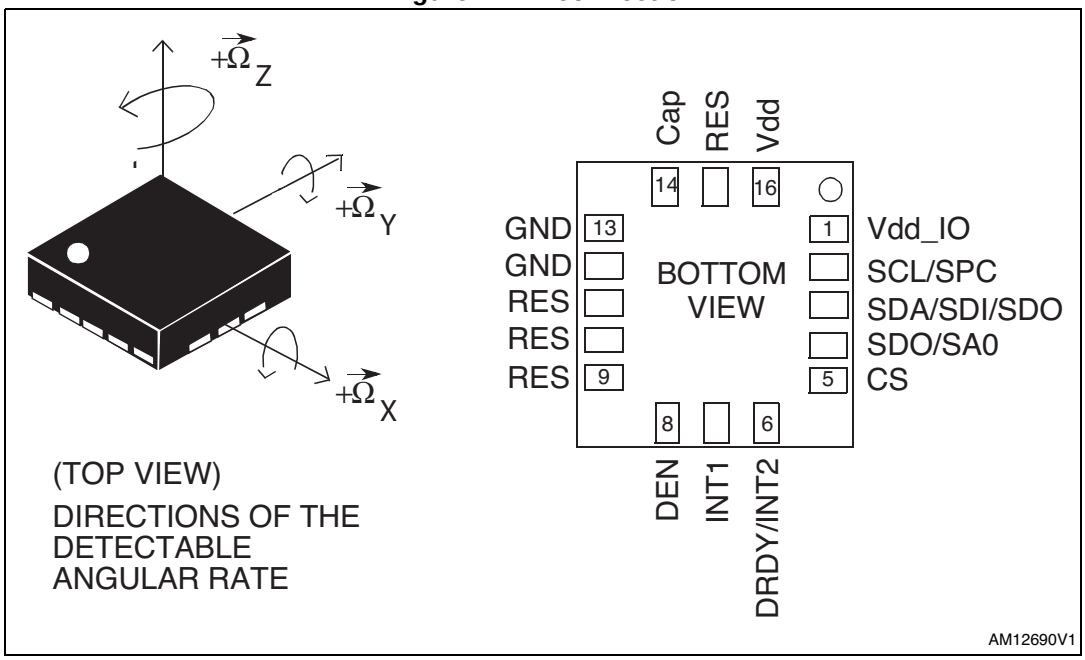


Table 2. Pin description

Pin#	Name	Function
1	Vdd_IO(1)	Power supply for I/O pins
2	SCL SPC	I²C serial clock (SCL) SPI serial port clock (SPC)
3	SDA SDI SDO	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
4	SDO SA0	SPI serial data output (SDO) I²C less significant bit of the device address (SA0)
5	CS	I²C/SPI mode selection (1: SPI idle mode / I²C communication enabled; 0: SPI communication mode / I2C disabled)
6	DRDY/INT2	Data ready/fifo interrupt (FIFO threshold/overrun/empty)
7	INT1	Programmable interrupt
8	DEN(2)	Gyroscope data enable
9	Reserved	Connect to GND
10	Reserved	Connect to GND
11	Reserved	Connect to GND or VDD
12	GND	0 V supply
13	GND	0 V supply
14	Cap	Connect to GND with ceramic capacitor(3)
15	Reserved	Connect to GND or VDD
16	Vdd(4)	Power supply

1. Recommended 100 nF filter capacitor.
2. Connected to GND if DEN is not used.
3. 10 nF (+/-10%), 25 V. 1 nF minimum value has to be guaranteed under 12 V bias condition.
4. Recommended 100 nF plus 10 µF capacitors.

2 Mechanical and electrical specifications

2.1 Mechanical characteristics

@ Vdd = 3.0 V, T = 25 °C unless otherwise noted[a].

Table 3. Mechanical characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
FS	Measurement range	User selectable		±245 ±500 ±2000		dps
So	Sensitivity			8.75 17.50 70.00		mdps/digit
SoDr	Sensitivity change vs. temperature[2]	From -40 °C to +85 °C Delta from T = 25 °C		±2		%
DVoff	Digital Zero-rate level	FS = 2000 dps		±25		dps
OffDr	Zero-rate level change vs temperature[3]	FS = 2000 dps		±0.04		dps/°C
NL	Non linearity[3]	Best fit straight line		0.2		% FS
Rn	Rate noise density[3]	BW = 50 Hz		0.011		dps/($\sqrt{Hz}$)
ODR	Digital output data rate[3]			11.9/23.7/ 47.3/94.7/ 189.4/ 378.8/ 757.6		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. Guaranteed by design.
3. The period (1/ODR), length of time between two consecutive sampling, must be derived by the reciprocal of the maximum. and minimum ODR limits: for example for ODR = 189.4 Hz, sampling period range will be within [4591 µs, 6211 µs] (where ODR minimum and maximum have been approximated at 162 Hz, 219 Hz respectively).

a. The product is factory calibrated at 3.0 V. The operational power supply range is specified in *Table 4*.

2.2 Electrical characteristics

@ Vdd =3.0 V, T=25 °C unless otherwise noted[b].

Table 4. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
Vdd	Supply voltage		2.2	3.0	3.6	V
Vdd_IO	I/O pins supply voltage[2]		1.71		Vdd+0.1	V
Idd	Supply current			5.0		mA
IddSL	Supply current in sleep mode[3]	Selectable by digital interface		2.5		mA
IddPdn	Supply current in power-down mode	Selectable by digital interface		1		µA
VIH	Digital high level input voltage		0.8*Vdd_IO			V
VIL	Digital low level input voltage				0.2*Vdd_IO	V
Ton	Turn-on time[4]	LPF2 disabled ODR = 190 Hz		50		ms
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.
2. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses, in this condition the measurement chain is powered off.
3. Sleep mode introduces a faster turn-on time related to power down mode.
4. Time to obtain stable sensitivity (within ±5% of final value) after exiting power-down mode. It is guaranteed by design.

b. The product is factory calibrated at 3.0 V.

2.3 Temperature sensor characteristics

@ Vdd =3.0 V, T=25 °C unless otherwise noted[c].

Table 5. Temperature sensor characteristics

Symbol	Parameter	Test condition	Min.	Typ.[1]	Max.	Unit
TSDr	Temperature sensor output change vs temperature	-		-1		°C/digit
TODR	Temperature refresh rate			1		Hz
Top	Operating temperature range		-40		+85	°C

1. Typical specifications are not guaranteed.

c. The product is factory calibrated at 3.0 V.

2.4 Communication interface characteristics

2.4.1 SPI - serial peripheral interface

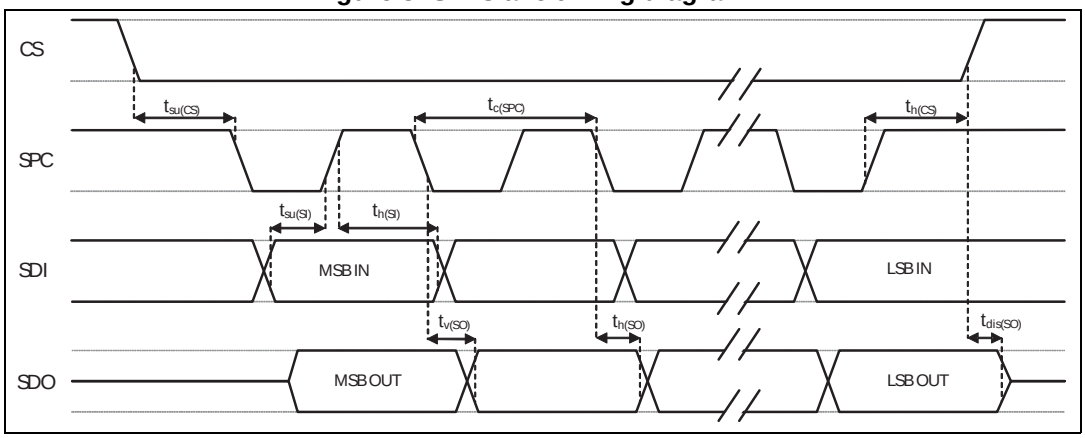
Subject to general operating conditions for Vdd and Top.

Table 6. SPI slave timing values

Symbol	Parameter	Value(1)		Unit
		Min.	Max.	
tc(SPC)	SPI clock cycle	100		ns
fc(SPC)	SPI clock frequency		10	MHz
tsu(CS)	CS setup time	5		ns
th(CS)	CS hold time	20		
tsu(SI)	SDI input setup time	5		
th(SI)	SDI input hold time	15		
tv(SO)	SDO valid output time		50	
th(SO)	SDO output hold time	5		
tdis(SO)	SDO output disable time		50	

1. Values are guaranteed at 10 MHz clock frequency for SPI with both 4 and 3 wires, based on characterization results, not tested in production.

Figure 3. SPI slave timing diagram(d)



d. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both Input and Output port.

2.4.2 I²C - Inter IC control interface

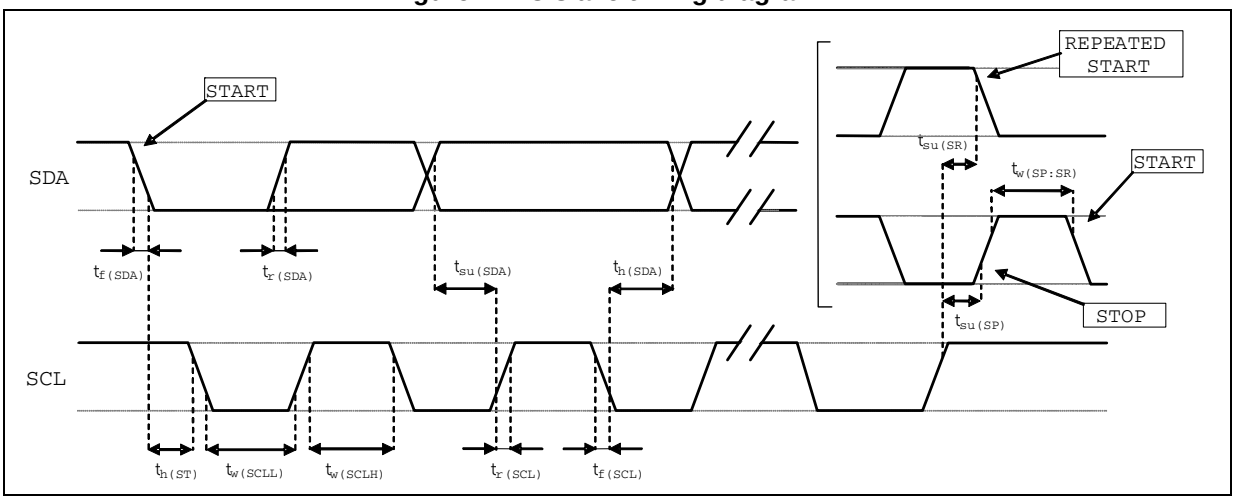
Subject to general operating conditions for Vdd and Top.

Table 7. I²C slave timing values

Symbol	Parameter	I²C standard mode(1)		I²C fast mode (1)		Unit
		Min.	Max.	Min.	Max.	
$f_{(SCL)}$	SCL clock frequency	0	100	0	400	kHz
$t_{w(SCLL)}$	SCL clock low time	4.7		1.3		μs
$t_{w(SCLH)}$	SCL clock high time	4.0		0.6		
$t_{su(SDA)}$	SDA setup time	250		100		ns
$t_{h(SDA)}$	SDA data hold time	0	3.45	0	0.9	μs
$t_{r(SDA)}$ $t_{r(SCL)}$	SDA and SCL rise time		1000	$20 + 0.1C_b$ (2)	300	ns
$t_{f(SDA)}$ $t_{f(SCL)}$	SDA and SCL fall time		300	$20 + 0.1C_b$ (2)	300	
$t_{h(ST)}$	START condition hold time	4		0.6		μs
$t_{su(SR)}$	Repeated START condition setup time	4.7		0.6		
$t_{su(SP)}$	STOP condition setup time	4		0.6		
$t_{w(SP:SR)}$	Bus free time between STOP and START condition	4.7		1.3		

1. Data based on standard I²C protocol requirement, not tested in production.
2. Cb = total capacitance of one bus line, in pF.

Figure 4. I²C slave timing diagram(e)



e. Measurement points are done at 0.2·Vdd_IO and 0.8·Vdd_IO, for both ports.

2.5 Absolute maximum ratings

Stresses above those listed as “Absolute maximum ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device under these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute maximum ratings

Symbol	Ratings	Maximum value	Unit
Vdd	Supply voltage	-0.3 to 4.8	V
T_{STG}	Storage temperature range	-40 to +125	°C
Sg	Acceleration g for 0.1 ms	10,000	g
ESD	Electrostatic discharge protection	2 (HBM)	kV
Vin	Input voltage on any control pin (including CS,SCL/SPC,SDA/SDI/SDO,SDO/SA0,DEN)	0.3 to Vdd_IO +0.3	V

Note: Supply voltage on any pin should never exceed 4.8 V.

This is a mechanical shock sensitive device, improper handling can cause permanent damage to the part.

This is an ESD sensitive device, improper handling can cause permanent damage to the part.

2.6 Terminology

2.6.1 Sensitivity

An angular rate gyroscope is a device that produces a positive-going analog output for counterclockwise rotation around the sensitive axis considered. Sensitivity describes the gain of the sensor and can be determined by applying a defined angular velocity to it. This value changes very little over temperature and time.

2.6.2 Zero-rate level

Zero-rate level describes the actual output signal if there is no angular rate present. Zero-rate level of precise MEMS sensors is, to some extent, a result of stress to the sensor and therefore zero-rate level can slightly change after mounting the sensor onto a printed circuit board or after exposing it to extensive mechanical stress.

2.7 Soldering information

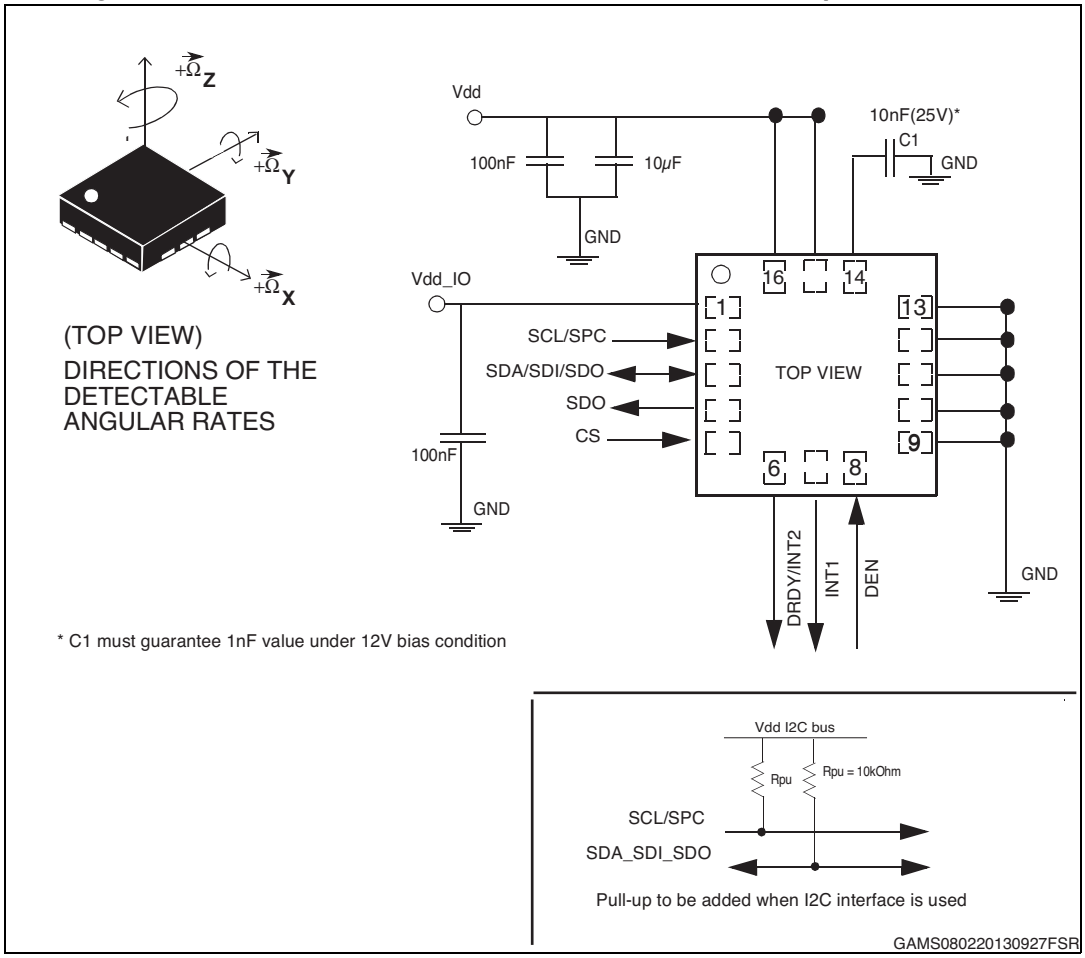
The LGA package is compliant with the ECOPACK®, RoHS and “Green” standard.
It is qualified for soldering heat resistance according to JEDEC J-STD-020.

Leave “Pin 1 Indicator” unconnected during soldering.

Land pattern and soldering recommendations are available at www.st.com/mems.

3 Application hints

Figure 5. L3GD20H electrical connections and external components values



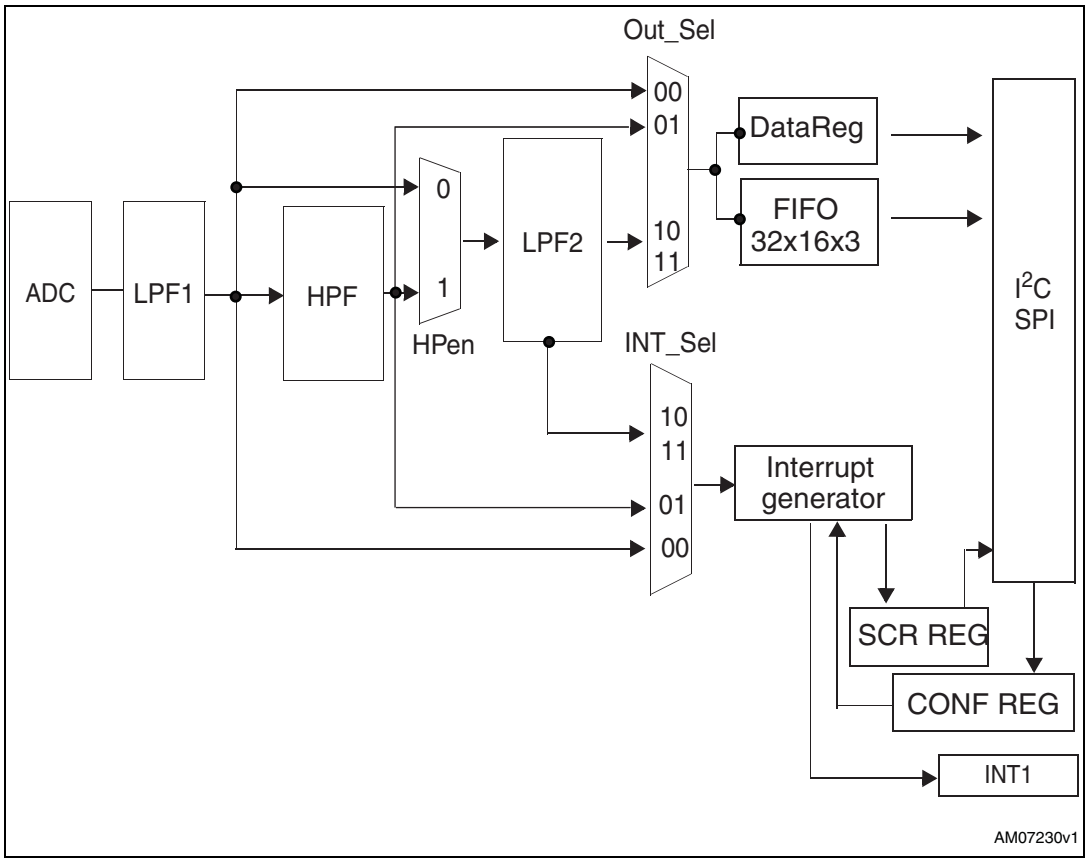
Power supply decoupling capacitors (100 nF + 10 μF) should be placed as near as possible to the device (common design practice).

If Vdd and Vdd_IO are not connected together, 100 nF and 10 μF decoupling capacitors must be placed between Vdd and common ground while 100 nF between Vdd_IO and common ground. Capacitors should be placed as near as possible to the device (common design practice).

4 Digital main blocks

4.1 Block diagram

Figure 6. Block diagram



4.2 FIFO

L3GD20H embeds 32 slots of 16-bit data FIFO for each of the three output channels: yaw, pitch and roll. This allows consistent power saving for the system, since the host processor does not need to continuously poll data from the sensor, but it can wakeup only when needed and burst the significant data out from the FIFO. This buffer can work accordingly to seven different modes: Bypass mode, FIFO-mode, Stream mode, Stream-to-FIFO mode, Bypass-to-Stream, Dynamic-Stream, Bypass-to-FIFO. Each mode is selected by the FM2:0 bits in FIFO_CTRL register. Programmable FIFO threshold level, FIFO empty or FIFO overrun events are available on FIFO_SRC register and can be set to generate dedicated interrupts on DRDY/INT2 pin.

FIFO_SRC(EMPTY) is equal to '1' when no samples are available.

FIFO_SRC(FTH) goes to '1' if a new data arrives and FIFO_SRC(FSS4:0) is greater than or equal to FIFO Threshold configured to FTH4:0 into FIFO_CTRL (2Eh). FIFO_SRC(FTH) goes to '0' if reading Yaw, Pitch and Roll data slot from FIFO and FIFO_SRC(FSS4:0) is minor than or equal to FIFO_CTRL(FTH4:0).

FIFO_SRC(OVRN) is equal to '1' if a FIFO slot is overwritten.

FIFO feature is enabled writing to '1' CTRL5(FIFO_EN).

To guarantee the switching into and out of FIFO mode discard the first sample aquired.

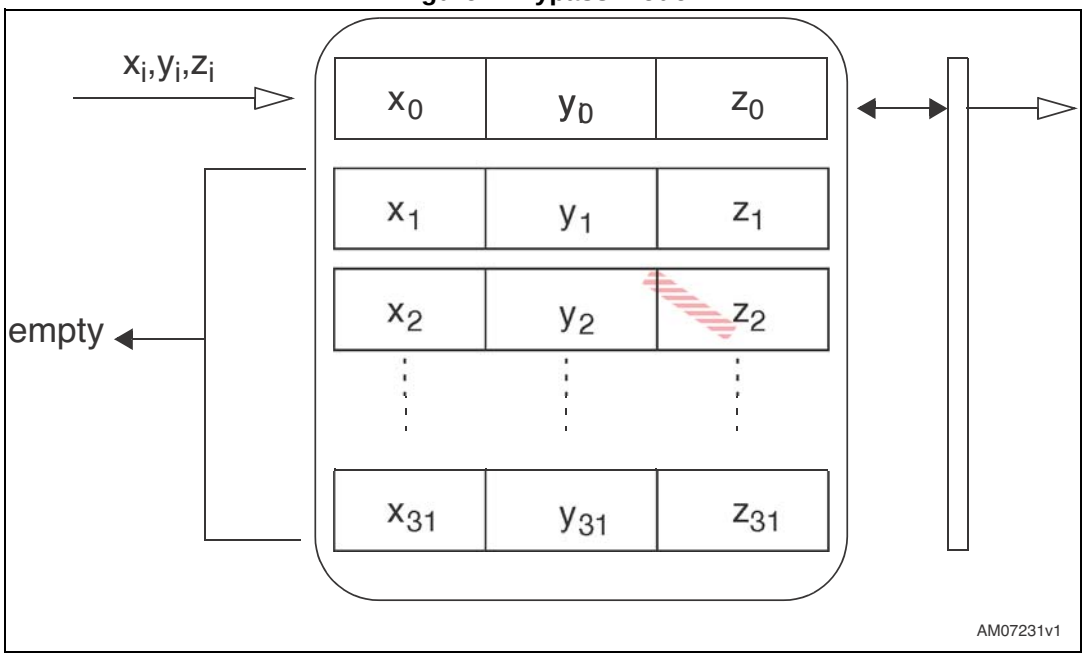
4.2.1 Bypass mode

In bypass mode (FIFO_CTRL(FM2:0) = 000), the FIFO is not operational and it remains empty.

Bypass mode is also used to reset the FIFO when in FIFO-mode.

As described in the next figure, for each channel only the first address is used. When a new data is available the old one is overwritten.

Figure 7. Bypass mode



4.2.2 FIFO mode

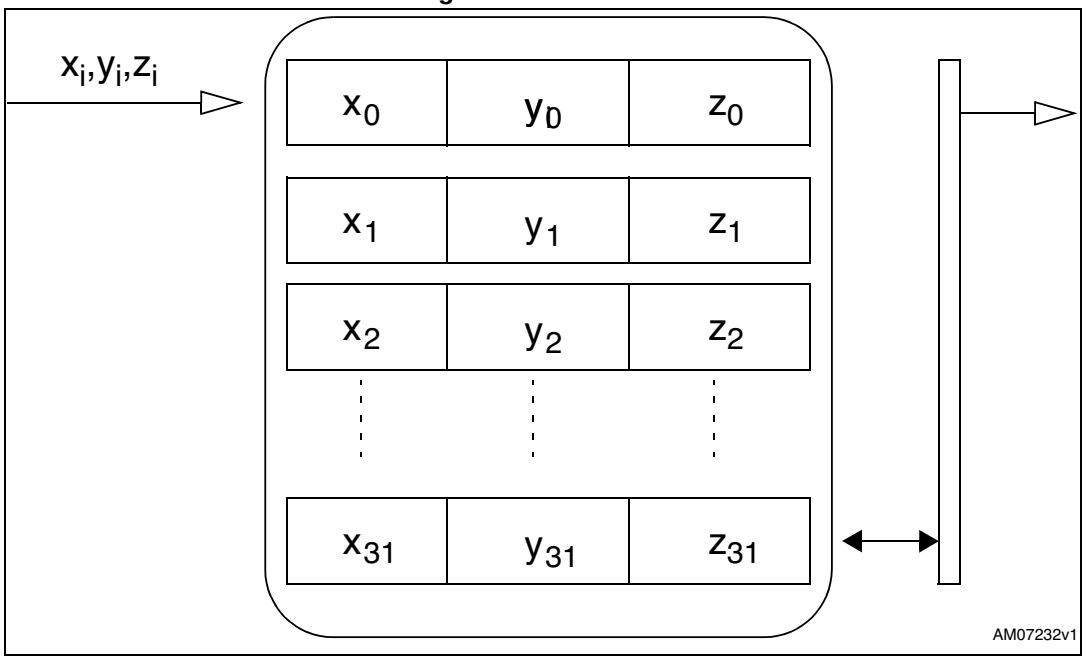
In FIFO mode (FIFO_CTRL(FM2:0) = 001) data from Yaw, Pitch and Roll channels are stored into the FIFO until it is full.

To reset FIFO content Bypass mode should be written in FIFO_CTRL(FM2:0) '000' value. After this reset command it is possible to restart FIFO mode writing FIFO_CTRL(FM2:0) the value '001'.

FIFO buffer can memorize 32 Yaw, Pitch and Roll data, but the depth of the FIFO can be reduced by means of CTRL5(StopOnFTH) bit setting to '1' StopOnFTH bit, FIFO depth is limited to FIFO_CTRL(FTH4:0) - 1.

A FIFO Threshold interrupt can be enabled (INT2_ORun bit into CTRL3 (22h)) in order to be raised when the FIFO is filled to the level specified into the FTH4:0 bits of FIFO_CTRL (2Eh). When FIFO Threshold interrupt occurs, the first data has been overwritten and the FIFO stops collecting data from the input channels.

Figure 8. FIFO mode

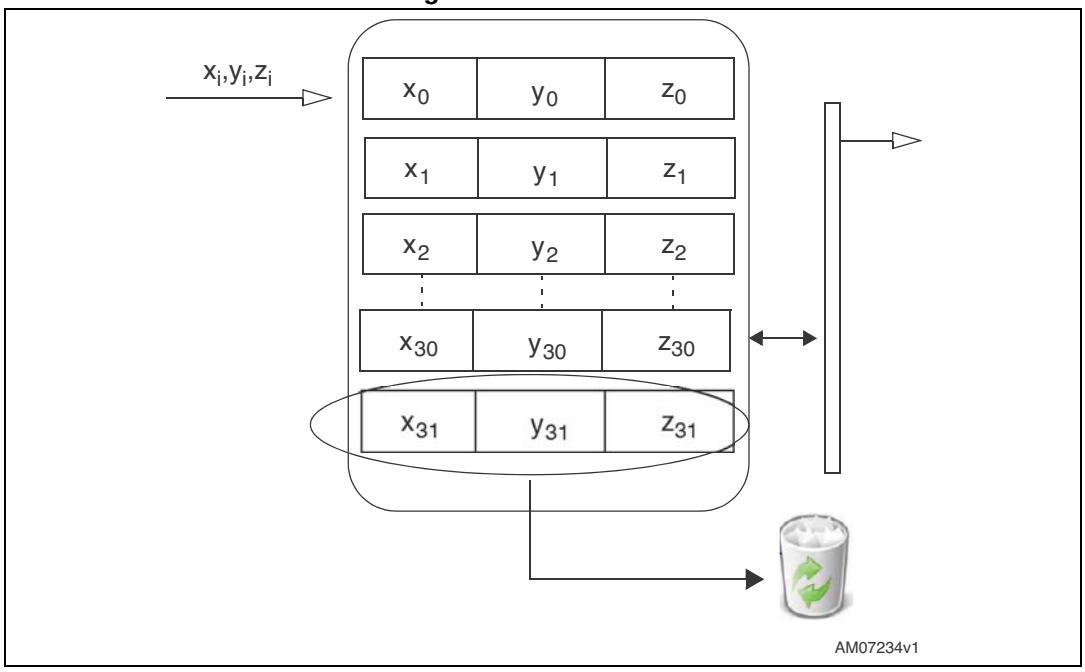


4.2.3 Stream mode - dynamic stream

Stream mode (FIFO_CTRL(FM2:0) = 010) provides continuous FIFO update: as new data arrives the older is discarded.

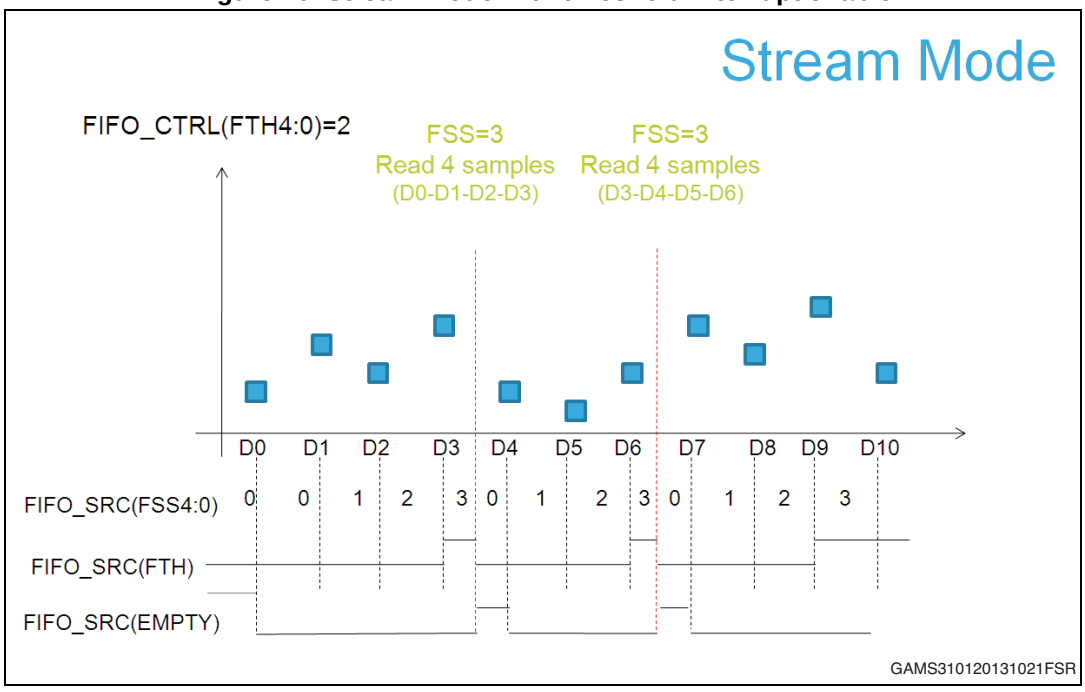
An overrun interrupt can be enabled, CTRL3(INT2_ORun)= '1', in order to read the whole FIFO content at once. If in the application no data can be lost and it is not possible to read at least one sample for each axis within one ODR period, a FIFO Threshold interrupt can be enabled in order to read partially the FIFO and let free memory slots for data incoming. Setting the FIFO_CTRL(FTH4:0) to N value, the number of Yaw, Pitch and Roll data samples that should be read at FIFO Threshold interrupt rising is up to (N+1).

Figure 9. Stream mode



In the latter case reading all FIFO content before an overrun interrupt has occurred, the first data read is equal to the last already read in previous burst, so the number of new data available in FIFO depends on previous reading (see FIFO_SRC behavior depicted in next figures).

Figure 10. Stream mode with threshold interrupt enable



In dynamic-stream mode (FIFO_CTRL(FM2:0) = 110) after emptying the FIFO the first new sample that arrives becomes the first to be read in subsequent read burst. In this way in

dynamic-stream mode (FIFO_CTRL(FM2:0) = 110) the number of new data available in FIFO does not depend on previous reading.

In dynamic-stream mode FIFO_SRC(FSS4:0) + 1 is the number of new X, Y and Z samples available in the FIFO buffer.

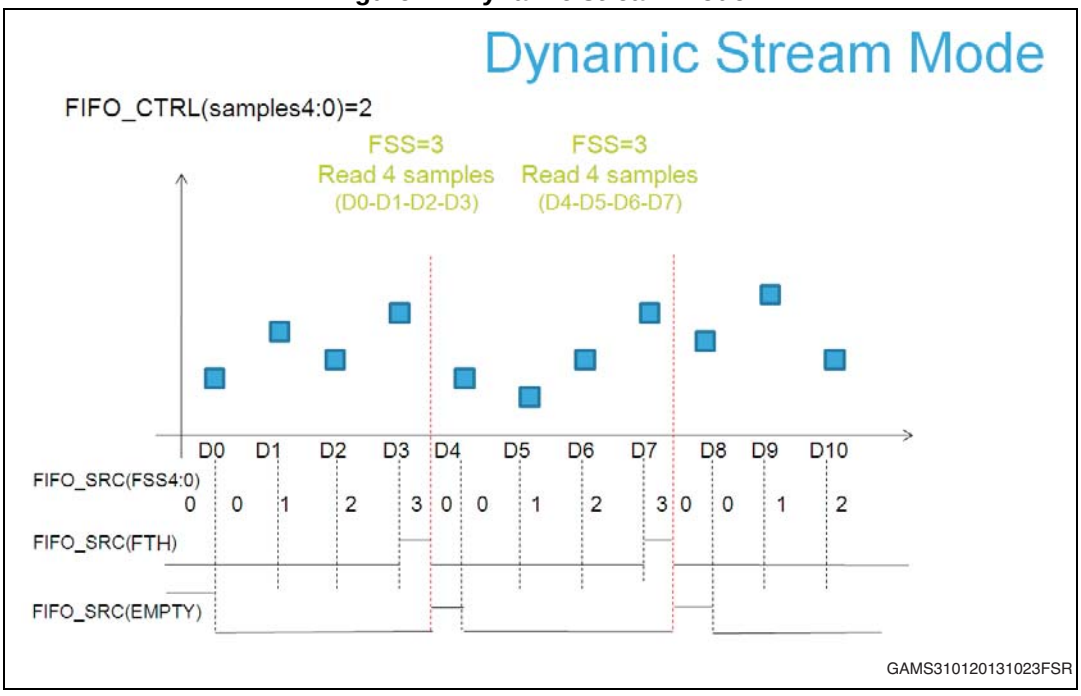
Stream mode is intended to be used reading all 32 samples of FIFO within an ODR after receiving an overrun signal.

Dynamic-stream is intended to be used to read FIFO_SRC(FSS4:0) + 1 samples when it is not possible to guarantee data reading within an ODR.

In dynamic-stream mode FIFO_CTRL(FTH4:0) setting should be between 1 and 30.

Also a FIFO Threshold interrupt CTRL3(INT2_FTH) can be enabled in order to read data from the FIFO and let free memory slot for data incoming. Setting the FIFO_CTRL(FTH4:0) to N value, the number of X, Y and Z data samples that should be read at FIFO Threshold interrupt rising, in order to read the whole FIFO content, is N + 2.

Figure 11. Dynamic stream mode



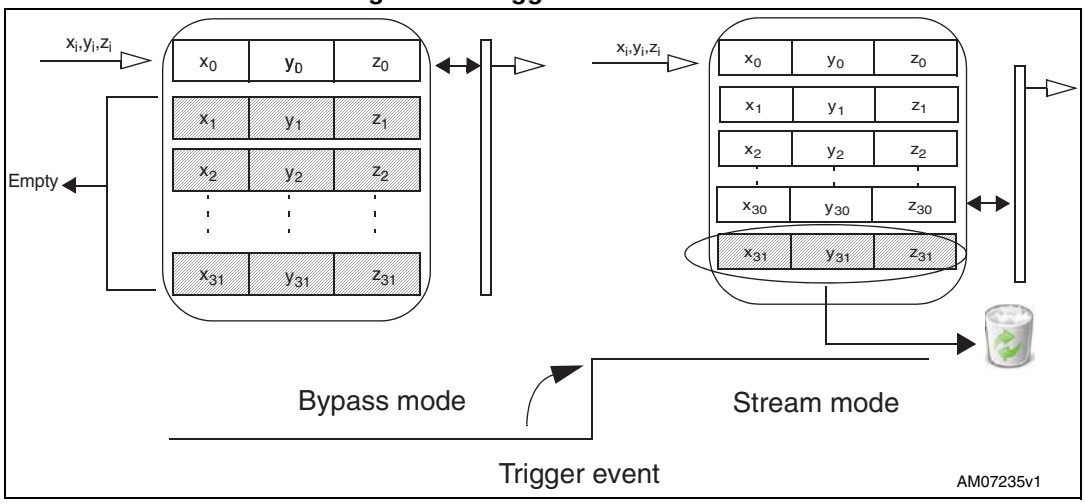
4.2.4 Stream-to-FIFO mode

In stream-to-FIFO mode (FIFO_CTRL(FM2:0) = 011), FIFO behavior changes according to IG_SRC(IA) bit. When IG_SRC(IA) bit is equal to '1' FIFO operates in FIFO-mode, when IG_SRC(IA) bit is equal to '0' FIFO operates in Stream mode.

Interrupt generator should be set to the desired configuration by means of IG_CFG, IG_THS_XH, IG_THS_XL, IG_THS_YH, IG_THS_YL, IG_THS_ZH and IG_THS_ZL.

IG_CFG(LIR) bit should be put to '1' in order to have latched interrupt.

Figure 12. Trigger stream mode



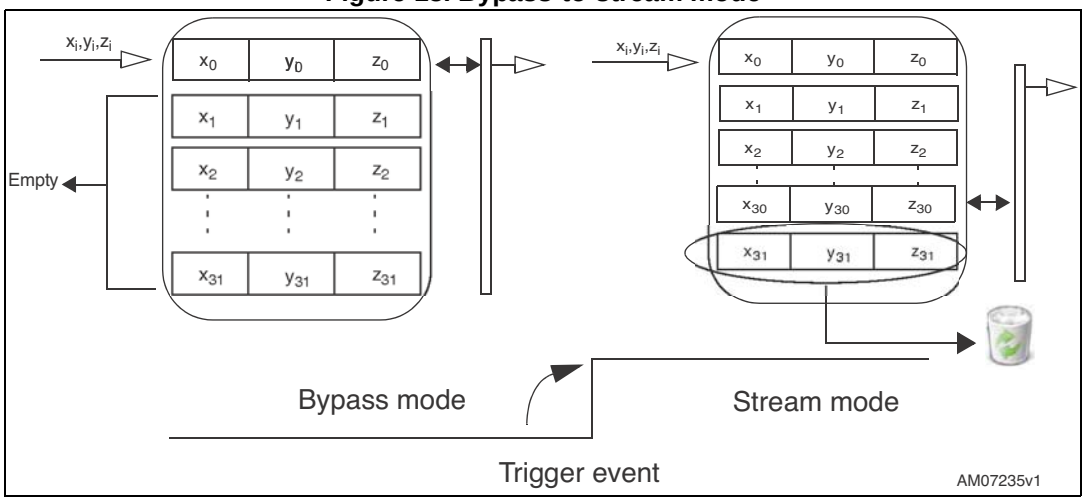
4.2.5 Bypass-to-stream mode

In bypass-to-stream mode (FIFO_CTRL(FM2:0) = '100'), Yaw, Pitch and Roll measurement storage inside FIFO operates in Stream mode when IG_SRC (IA) is equal to '1', otherwise FIFO content is reset (bypass mode) .

Interrupt generator should be set to the desired configuration by means of IG_CFG, IG_THS_XH, IG_THS_XL, IG_THS_YH, IG_THS_YL, IG_THS_ZH and IG_THS_ZL.

IG_CFG(LIR) bit should be put to '1' in order to have latched interrupt.

Figure 13. Bypass-to-stream mode



4.2.6 Bypass-to-FIFO mode

In bypass-to-FIFO mode (FIFO_CTRL(FM2:0) = '111', FIFO behavior changes according to IG_SRC(IA) bit. When IG_SRC(IA) bit is equal to '1' FIFO operates in FIFO-mode, when IG_SRC(IA) bit is equal to '0' FIFO operates in bypass mode (FIFO content reset). If a latched interrupt is generated FIFO starts collecting data until the first data into the FIFO-buffer is overwritten. Interrupt generator should be set to the desired configuration by means of IG_CFG, IG_THS_XH, IG_THS_XL, IG_THS_YH, IG_THS_YL, IG_THS_ZH and IG_THS_ZL.

IG_CFG (LIR) bit should be put to '1' in order to have latched interrupt.

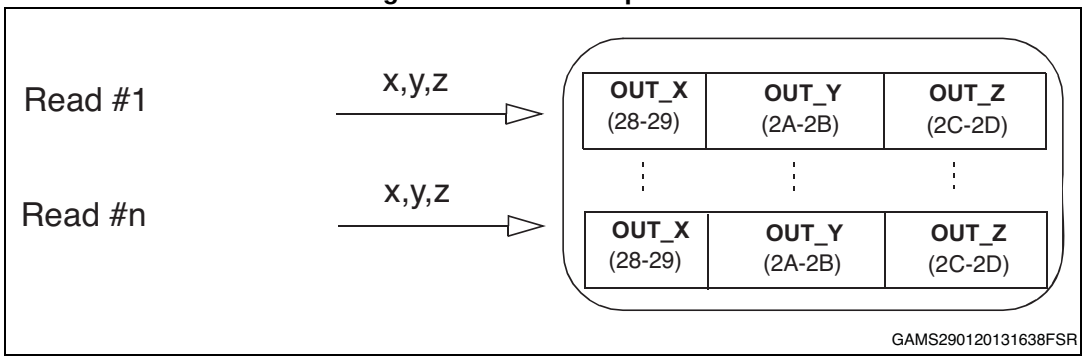
4.2.7 Retrieve data from FIFO

FIFO data is read through OUT_X_L and OUT_X_H (Addr reg 28h and 29h), OUT_Y_L OUT_Y_H (Addr reg 2Ah and 2Bh) and OUT_Z_L and OUT_Z_H (Addr reg 2Ch and 2Dh) registers. A read operation by means of serial interface of OUT_X, OUT_Y or OUT_Z output registers provides the data stored into the FIFO. Each time data is read from the FIFO, the oldest X, Y and Z data are placed into the OUT_X, OUT_Y and OUT_Z registers and both single read and read_burst operations can be used.

4.2.8 FIFO multiple read (burst)

Starting from the Addr 28h multiple read can be performed. Once the reading reaches the Addr 2Dh the system automatically restarts from the Addr. 28h.

Figure 14. FIFO multiple read



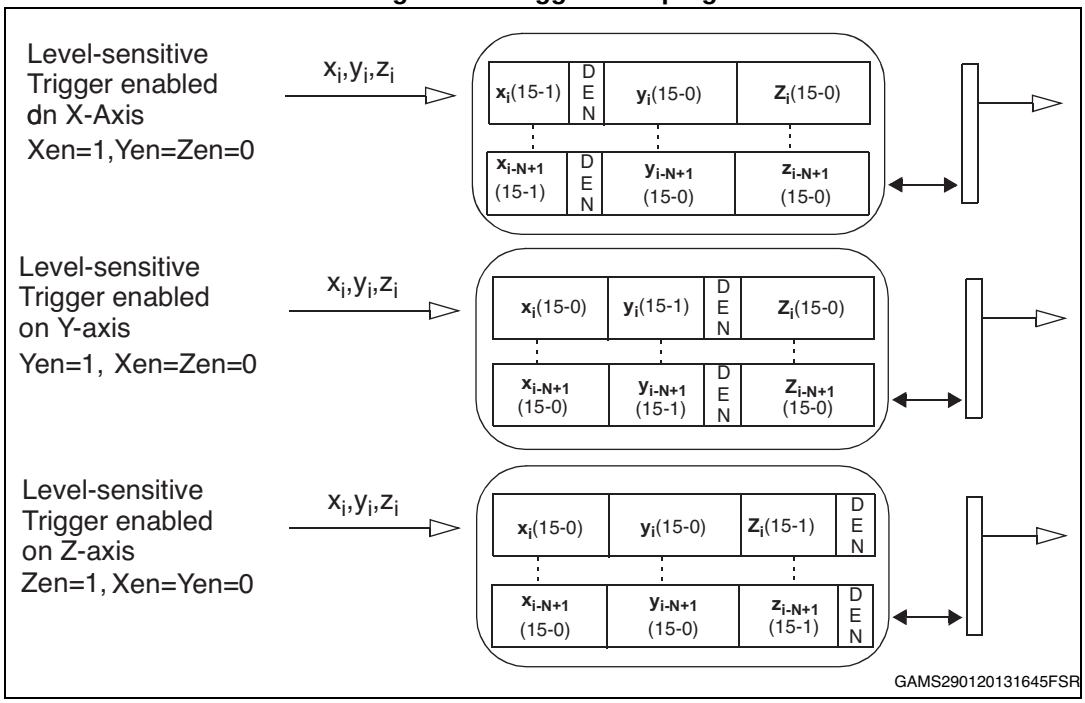
4.3 Level-sensitive/edge sensitive/impulse sensitive data enable

L3GD20H allows external trigger level recognition through enabling EXTRen and LVLen bits into CTRL2 (21h) and IMPen bit into CTRL4 (23h). Three different modes can be used: level, edge or impulse sensitive trigger.

Table 9. Trigger stamping mode

LVLen	EXTRen	IMPen	Trigger stamping mode
1	0	0	Level sensitive trigger
0	1	0	Edge sensitive trigger
1	0	1	Impulse sensitive trigger

Figure 15. Trigger stamping



4.3.1 Level sensitive trigger stamping

Level sensitive trigger can be enabled by setting to ‘1’ the LVLen bit into CTRL2 (21h) while EXTRen bit into CTRL2 (21h) and IMPen bit into CTRL4 (23h) have to be set to ‘0’.

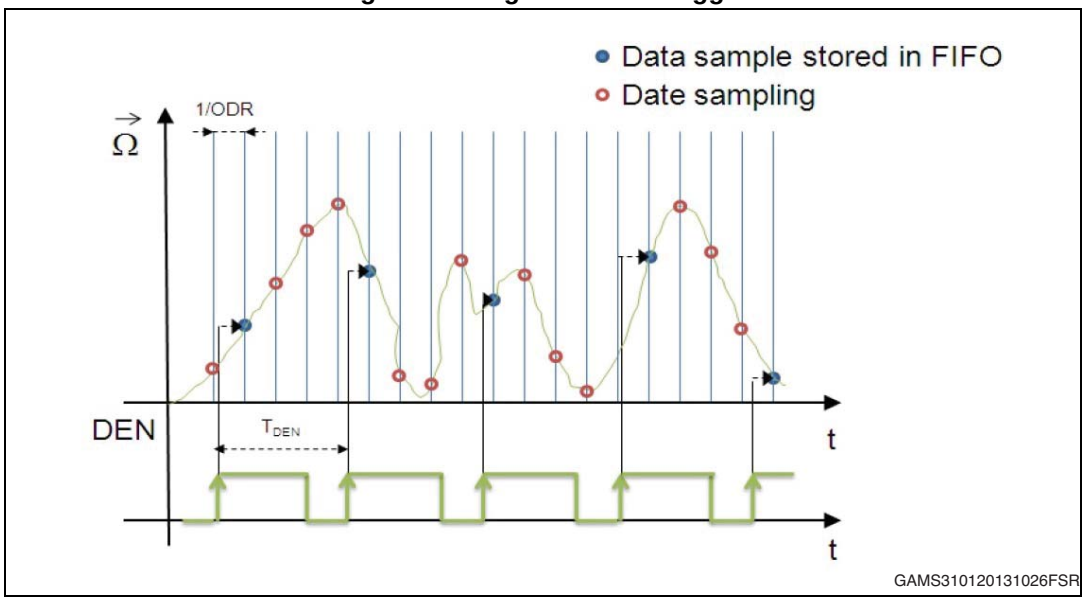
Once enabled, DEN level replaces the LSB of X, Y or Z axes configurable through Xen, Yen, Zen bits into CTRL1 (20h). Data is stored inside the FIFO with the internal selected ODR.

4.3.2 Edge sensitive trigger

Edge sensitive trigger can be enabled by setting to ‘1’ the EXTRen bit into CTRL2 (21h) while LVLen bit into CTRL2 (21h) and IMPen bit into CTRL4 (23h) have to be set to ‘0’.

Once enabled, FIFO is filled with the Pitch, Roll and Yaw data on the rising edge of DEN input signal. When ODR selected is 800 Hz, maximum DEN sample frequency is f_{DEN} =1/T_{DEN} = 400 Hz.

Figure 16. Edge-sensitive trigger



4.3.3 Impulse sensitive trigger

Impulse sensitive trigger can be enabled by setting to '1' LVLen bit into CTRL2 (21h) and IMPen bit into CTRL4 (23h) while the EXTRen bit into CTRL2 (21h) has to be set to '0'.

If the duration of the DEN pulse is shorter than the selected ODR, the Impulse sensitive trigger functionality has to be enabled.

5 Digital interfaces

The registers embedded inside the L3GD20H may be accessed through both the I^2C and SPI serial interfaces. The latter may be SW configured to operate either in 3-wire or 4-wire interface mode.

The serial interfaces are mapped onto the same pins. To select/exploit the I^2C interface, CS line must be tied high (i.e connected to Vdd_IO).

Table 10. Serial interface pin description

Pin name	Pin description
CS	SPI enable I^2C/SPI mode selection (1: I^2C mode; 0: SPI enabled)
SCL/SPC	I^2C Serial Clock (SCL) SPI Serial Port Clock (SPC)
SDA/SDI/SDO	I^2C Serial Data (SDA) SPI Serial Data Input (SDI) 3-wire Interface Serial Data Output (SDO)
SDO/SA0	SPI Serial Data Output (SDO) I^2C less significant bit of the device address

5.1 I^2C serial interface

The L3GD20H I^2C is a bus slave. The I^2C is employed to write data into registers whose content can also be read back.

The relevant I^2C terminology is given in the table below.

Table 11. I^2C terminology

Term	Description
Transmitter	The device which sends data to the bus
Receiver	The device which receives data from the bus
Master	The device which initiates a transfer, generates clock signals and terminates a transfer
Slave	The device addressed by the master

There are two signals associated with the I^2C bus: the serial clock line (SCL) and the serial data line (SDA). The latter is a bidirectional line used for sending and receiving the data to/from the interface. Both the lines must be connected to Vdd_IO through external pull-up resistor. When the bus is free both the lines are high.

The I^2C interface is compliant with fast mode (400 kHz) I^2C standards as well as with the normal mode.

5.1.1 I²C operation

The transaction on the bus is started through a START (ST) signal. A START condition is defined as a HIGH to LOW transition on the data line while the SCL line is held HIGH. After this has been transmitted by the Master, the bus is considered busy. The next byte of data transmitted after the start condition contains the address of the slave in the first 7 bits and the eighth bit tells whether the Master is receiving data from the slave or transmitting data to the slave. When an address is sent, each device in the system compares the first seven bits after a start condition with its address. If they match, the device considers itself addressed by the Master.

The Slave ADdress (SAD) associated to the L3GD20H is 110101xb. SDO/SA0 pin can be used to modify less significant bit of the device address. If SDO/SA0 pin is connected to voltage supply LSb is ‘1’ (address 1101011b) else if SDO/SA0 pin is connected to ground LSb value is ‘0’ (address 1101010b). This solution permits to connect and address two different gyroscopes to the same I²C bus.

Data transfer with acknowledge is mandatory. The transmitter must release the SDA line during the acknowledge pulse. The receiver must then pull the data line LOW so that it remains stable low during the HIGH period of the acknowledge clock pulse. A receiver which has been addressed is obliged to generate an acknowledge after each byte of data received.

The I²C embedded inside the L3GD20H behaves like a slave device and the following protocol must be adhered to. After the start condition (ST) a slave address is sent, once a slave acknowledge (SAK) has been returned, a 8-bit sub-address will be transmitted: the 7 LSb represent the actual register address while the MSB enables address auto increment. If the MSb of the SUB field is 1, the SUB (register address) will be automatically incremented to allow multiple data read/write.

The slave address is completed with a Read/Write bit. If the bit was ‘1’ (Read), a repeated START (SR) condition will have to be issued after the two sub-address bytes; if the bit is ‘0’ (Write) the Master will transmit to the slave with direction unchanged. *Table 12* explains how the SAD+Read/Write bit pattern is composed, listing all the possible configurations.

Table 12. SAD+Read/Write patterns

Command	SAD[6:1]	SAD[0] = SDO	R/W	SAD+R/W
Read	110101	0	1	11010101 (D5h)
Write	110101	0	0	11010100 (D4h)
Read	110101	1	1	11010111 (D7h)
Write	110101	1	0	11010110 (D6h)

Table 13. Transfer when Master is writing one byte to slave

Master	ST	SAD + W		SUB		DATA		SP
Slave			SAK		SAK		SAK	

Table 14. Transfer when Master is writing multiple bytes to slave

Master	ST	SAD + W		SUB		DATA		DATA		SP
Slave			SAK		SAK		SAK		SAK	

Table 15. Transfer when Master is receiving (reading) one byte of data from slave

Master	ST	SAD + W		SUB		SR	SAD + R			NMAK	SP
Slave			SAK		SAK			SAK	DATA		

Table 16. Transfer when Master is receiving (reading) multiple bytes of data from slave

Master	ST	SAD+W		SUB		SR	SAD+R			MAK		MAK		NMAK	SP
Slave			SAK		SAK			SAK	DATA		DATA		DATA		

Data are transmitted in byte format (DATA). Each data transfer contains 8 bits. The number of bytes transferred per transfer is unlimited. Data is transferred with the Most Significant bit (MSb) first. If a receiver can't receive another complete byte of data until it has performed some other function, it can hold the clock line, SCL LOW to force the transmitter into a wait state. Data transfer only continues when the receiver is ready for another byte and releases the data line. If a slave receiver doesn't acknowledge the slave address (i.e. it is not able to receive because it is performing some real time function) the data line must be left HIGH by the slave. The Master can then abort the transfer. A LOW to HIGH transition on the SDA line while the SCL line is HIGH is defined as a STOP condition. Each data transfer must be terminated by the generation of a STOP (SP) condition.

In order to read multiple bytes, it is necessary to assert the most significant bit of the sub-address field. In other words, SUB(7) must be equal to 1 while SUB(6-0) represents the address of first register to be read.

In the presented communication format MAK is Master Acknowledge and NMAK is No Master Acknowledge.

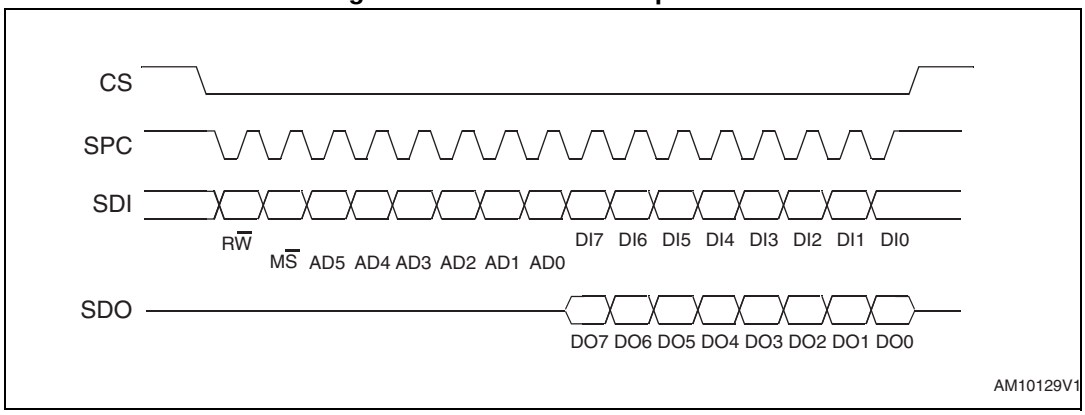
In order to disable the I2C block it is needed to write '1' in bit 3 of register located in address 39h.

5.2 SPI bus interface

The SPI is a bus slave. The SPI allows to write and read the registers of the device.

The Serial Interface interacts with the outside world with 4 wires: **CS**, **SPC**, **SDI** and **SDO**.

Figure 17. Read and write protocol



CS is the Serial Port Enable and it is controlled by the SPI master. It goes low at the start of the transmission and goes back high at the end. **SPC** is the Serial Port Clock and it is controlled by the SPI master. It is stopped high when **CS** is high (no transmission). **SDI** and **SDO** are respectively the Serial Port Data Input and Output. Those lines are driven at the falling edge of **SPC** and should be captured at the rising edge of **SPC**.

Both the Read Register and Write Register commands are completed in 16 clock pulses or in multiple of 8 in case of multiple bytes read/write. Bit duration is the time between two falling edges of **SPC**. The first bit (bit 0) starts at the first falling edge of **SPC** after the falling edge of **CS** while the last bit (bit 15, bit 23, ...) starts at the last falling edge of **SPC** just before the rising edge of **CS**.

bit 0: R$\overline{W}$ bit. When 0, the data DI(7:0) is written into the device. When 1, the data DO(7:0) from the device is read. In latter case, the chip will drive **SDO** at the start of bit 8.

bit 1: M$\overline{S}$ bit. When 0, the address will remain unchanged in multiple read/write commands. When 1, the address will be auto incremented in multiple read/write commands.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written into the device (MSb first).

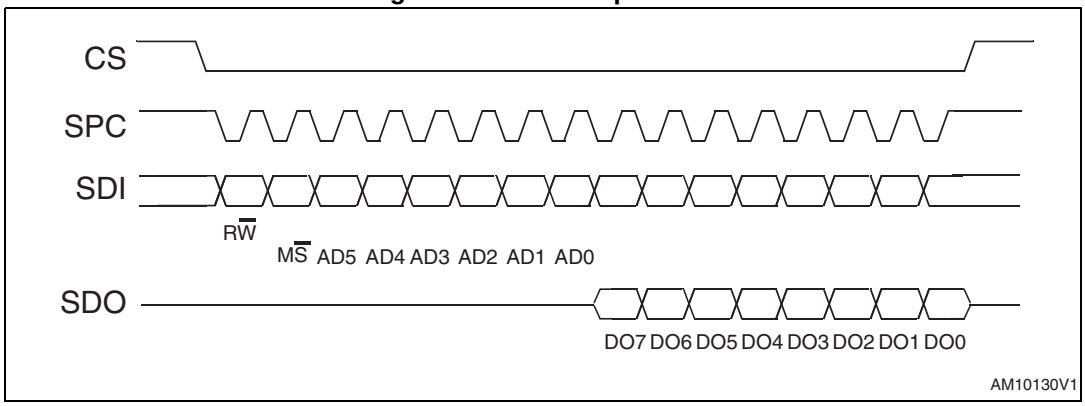
bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

In multiple read/write commands further blocks of 8 clock periods will be added. When M$\overline{S}$ bit is 0 the address used to read/write data remains the same for every block. When M$\overline{S}$ bit is 1 the address used to read/write data is incremented at every block.

The function and the behavior of **SDI** and **SDO** remain unchanged.

5.2.1 SPI read

Figure 18. SPI read protocol



The SPI Read command is performed with 16 clock pulses. Multiple byte read command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: READ bit. The value is 1.

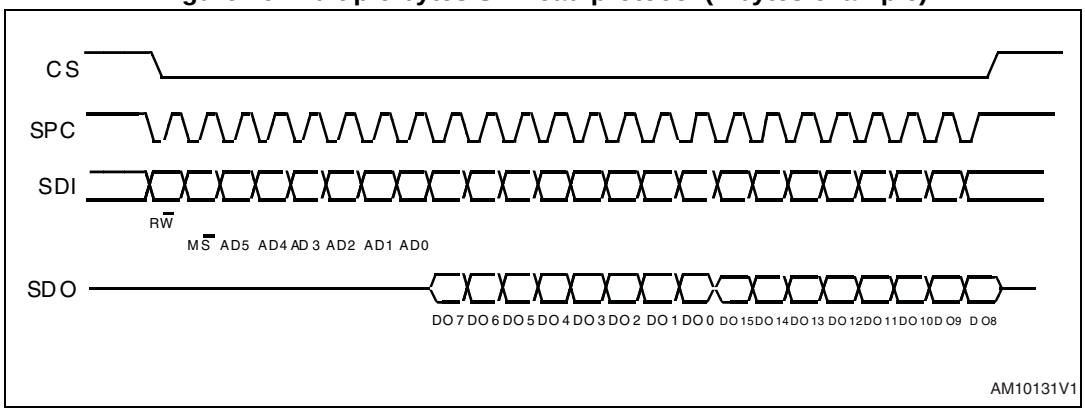
bit 1: MS bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

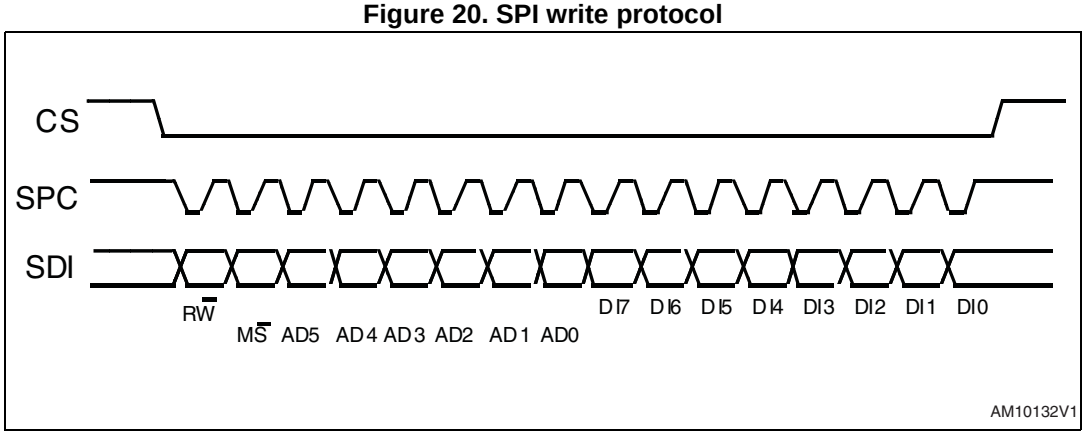
bit 16-... : data DO(...-8). Further data in multiple byte reading.

Figure 19. Multiple bytes SPI read protocol (2 bytes example)



5.2.2 SPI write

Figure 20. SPI write protocol



The SPI Write command is performed with 16 clock pulses. Multiple byte write command is performed adding blocks of 8 clock pulses at the previous one.

bit 0: WRITE bit. The value is 0.

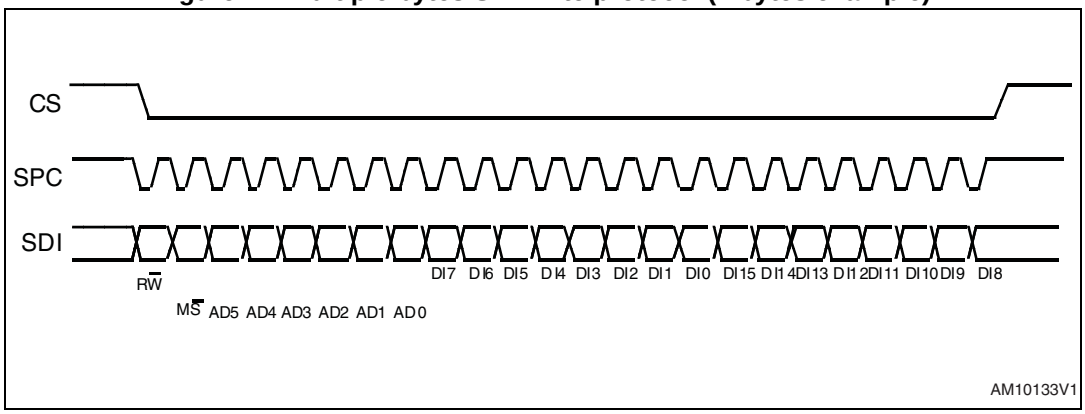
bit 1: M$\overline{S}$ bit. When 0 do not increment address, when 1 increment address in multiple writing.

bit 2 -7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DI(7:0) (write mode). This is the data that will be written inside the device (MSb first).

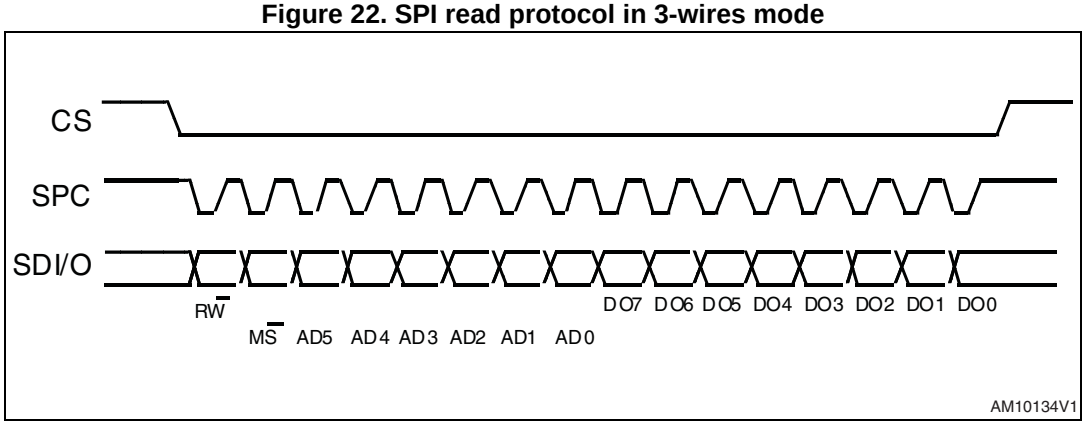
bit 16-... : data DI(...-8). Further data in multiple byte writing.

Figure 21. Multiple bytes SPI write protocol (2 bytes example)



5.2.3 SPI read in 3-wires mode

Figure 22. SPI read protocol in 3-wires mode



The SPI Read command is performed with 16 clock pulses:

bit 0: READ bit. The value is 1.

bit 1: $M\overline{S}$ bit. When 0 do not increment address, when 1 increment address in multiple reading.

bit 2-7: address AD(5:0). This is the address field of the indexed register.

bit 8-15: data DO(7:0) (read mode). This is the data that will be read from the device (MSb first).

Multiple read command is also available in 3-wires mode.

6 Output register mapping

The table given below provides a listing of the 8 bit registers embedded in the device and the related addresses:

Table 17. Register address map

Name	Type	Register address		Default
		Hex	Binary	
Reserved	-	00-0E	-	-
WHO_AM_I	r	0F	000 1111	11010111
Reserved	-	10-1F	-	-
CTRL1	rw	20	010 0000	00000111
CTRL2	rw	21	010 0001	00000000
CTRL3	rw	22	010 0010	00000000
CTRL4	rw	23	010 0011	00000000
CTRL5	rw	24	010 0100	00000000
REFERENCE	rw	25	010 0101	00000000
OUT_TEMP	r	26	010 0110	Output
STATUS	r	27	010 0111	Output
OUT_X_L	r	28	010 1000	Output
OUT_X_H	r	29	010 1001	Output
OUT_Y_L	r	2A	010 1010	Output
OUT_Y_H	r	2B	010 1011	Output
OUT_Z_L	r	2C	010 1100	Output
OUT_Z_H	r	2D	010 1101	Output
FIFO_CTRL	rw	2E	010 1110	00000000
FIFO_SRC	r	2F	010 1111	Output
IG_CFG	rw	30	011 0000	00000000
IG_SRC	r	31	011 0001	Output
IG_THS_XH	rw	32	011 0010	00000000
IG_THS_XL	rw	33	011 0011	00000000
IG_THS_YH	rw	34	011 0100	00000000
IG_THS_YL	rw	35	011 0101	00000000
IG_THS_ZH	rw	36	011 0110	00000000
IG_THS_ZL	rw	37	011 0111	00000000
IG_DURATION	rw	38	011 1000	00000000
LOW_ODR	rw	39	011 1001	00000000

Registers marked as *Reserved* must not be changed. The writing to those registers may cause permanent damages to the device.

The content of the registers that are loaded at boot should not be changed. They contain the factory calibration values. Their content is automatically restored when the device is powered-up.

7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve angular rate data. The registers address, made of 7 bits, is used to identify them and to write the data through serial interface.

7.1 WHO_AM_I (0Fh)

Table 18. WHO_AM_I register

1	1	0	1	0	1	1	1

Device identification register.

7.2 CTRL1 (20h)

Table 19. CTRL1 register(1)

DR1	DR0	BW1	BW0	PD	Zen	Xen	Yen

1. Xen, Yen, Zen enable X, Yor Z register in level sensitive trigger mode. Once LVLen bit = 1, DEN level replaces the LSB of X, Y or Z axes and all axis are available for reading.

Table 20. CTRL1 description

DR1-DR0	Output data rate selection. Refer to *Table 21*
BW1-BW0	Bandwidth selection. Refer to *Table 21*
PD	Power mode. Default value: 0. Refer to *Table* 0= Power Down 1= Normal Mode (For Sleep Mode set {PD:Zen:Yen:Xen} to {1000})
Zen	Z axis enable. Default value: 1 (0: Z axis disabled; 1: Z axis enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled; 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

DR<1:0> is used to set ODR selection. **BW <1:0>** is used to set bandwidth selection.

In the following table are reported all frequency resulting in combination of DR / BW bits.

Table 21. DR and BW configuration setting

Low_ODR(1)	DR <1:0>	BW <1:0>	ODR [Hz]	Cut-Off [Hz](2)
1	00	00	12.5	n.a.
1	00	01	12.5	n.a.
1	00	10	12.5	n.a.
1	00	11	12.5	n.a.
1	01	00	25	n.a.
1	01	01	25	n.a.
1	01	10	25	n.a.
1	01	11	25	n.a.
1	1X	00	50	16.6
1	1X	01	50	16.6
1	1X	10	50	16.6
1	1X	11	50	16.6
0	00	00	100	12.5
0	00	01	100	25
0	00	10	100	25
0	00	11	100	25
0	01	00	200	12.5
0	01	01	200	-
0	01	10	200	-
0	01	11	200	70
0	10	00	400	20
0	10	01	400	25
0	10	10	400	50
0	10	11	400	110
0	11	00	800	30
0	11	01	800	35
0	11	10	800	-
0	11	11	800	100

1. this bit is described in register LOW_ODR (39h register).
2. values in the table are indicative and they can vary proportionally with the specific ODR value.

Combination of **PD, Zen, Yen, Xen** are used to set device in different modes (power down / normal / sleep mode) according with the following table.

Table 22. Power mode selection configuration

Mode	PD	Zen	Yen	Xen
Power down	0	-	-	-
Normal	1	-	-	-
Sleep	1	0	0	0

7.3 CTRL2 (21h)

Table 23. CTRL2 register

EXTRen	LVLen	HPM1	HPM0	HPCF3	HPCF2	HPCF1	HPCF0

Table 24. CTRL2 description

EXTRen	Edge sensitive trigger Enable: Default value: 0 (0: external trigger disabled; 1: External trigger enabled)
LVLen	Level sensitive trigger Enable: Default value: 0 (0: level sensitive trigger disabled; 1: level sensitive trigger enabled)
HPM1-HPM0	High Pass filter Mode Selection. Default value: 00 Refer to *Table 25*
HPCF3-HPCF0	High Pass filter Cut Off frequency selection. Default value: 0000 Refer to *Table 26*

Table 25. High pass filter mode configuration

HPM1	HPM0	High pass filter mode
0	0	Normal mode (reset reading REFERENCE 25h register)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset on interrupt event

Table 26. High pass filter cut off frequency configuration [Hz](1)

HPCF3-0	ODR=12.5 Hz	ODR=25 Hz	ODR=50 Hz	ODR =100 Hz	ODR =200 Hz	ODR =400 Hz	ODR =800 Hz
0000	1	2	4	8	15	30	56
0001	0.5	1	2	4	8	15	30
0010	0.2	0.5	1	2	4	8	15
0011	0.1	0.2	0.5	1	2	4	8

Table 26. High pass filter cut off frequency configuration [Hz](1) (continued)

HPCF3-0	ODR=12.5 Hz	ODR=25 Hz	ODR=50 Hz	ODR =100 Hz	ODR =200 Hz	ODR =400 Hz	ODR =800 Hz
0100	0.05	0.1	0.2	0.5	1	2	4
0101	0.02	0.05	0.1	0.2	0.5	1	2
0110	0.01	0.02	0.05	0.1	0.2	0.5	1
0111	0.005	0.01	0.02	0.05	0.1	0.2	0.5
1000	0.002	0.005	0.01	0.02	0.05	0.1	0.2
1001	0.001	0.002	0.005	0.01	0.02	0.05	0.1

1. values in the table are indicative and they can vary proportionally with the specific ODR value

7.4 CTRL3 (22h)

Table 27. CTRL3 register

INT1_IG	INT1_Boot	H_Lactive	PP_OD	INT2_DRDY	INT2_FTH	INT2_ORun	INT2_Empty

Table 28. CTRL3 description

INT1_IG	Interrupt enable on INT1 pin. Default value 0. (0: disable; 1: enable)
INT1_Boot	Boot status available on INT1 pin. Default value 0. (0: disable; 1: enable)
H_Lactive	Interrupt active configuration on INT. Default value 0. (0: high; 1:low)
PP_OD	Push- Pull / Open drain. Default value: 0. (0: push-pull; 1: open drain)
INT2_DRDY	Date Ready on DRDY/INT2 pin. Default value 0. (0: disable; 1: enable)
INT2_FTH	FIFO Threshold interrupt on DRDY/INT2 pin. Default value: 0. (0: disable; 1: enable)
INT2_ORun	FIFO Overrun interrupt on DRDY/INT2 pin. Default value: 0. (0: disable; 1: enable)
INT2_Empty	FIFO Empty interrupt on DRDY/INT2 pin. Default value: 0. (0: disable; 1: enable)

7.5 CTRL4 (23h)

Table 29. CTRL4 register

BDU	BLE	FS1	FS0	IMPen	ST2	ST1	SIM

Table 30. CTRL4 description

BDU	Block data update. Default value: 0 (0: continuos update; 1: output registers not updated until MSB and LSB reading)
BLE	Big/little endian data selection. Default value 0. (0: Data LSB @ lower address; 1: Data MSB @ lower address)

Table 30. CTRL4 description (continued)

FS1-FS0	Full scale selection. Default value: 00 (00: 245 dps; 01: 500 dps; 1x: 2000 dps)
IMPen	Level sensitive latched enable. Default value: 0 (0: level sensitive latched disabled; 1: level sensitive latched enabled)
ST2-ST1	Self-test enable. Default value: 00 00 = normal mode (default) 01 = self-test 0 (+) 10 = unused 11 = self-test 1(-)
SIM	SPI Serial Interface Mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface).

7.6 CTRL5 (24h)

Table 31. CTRL5 register

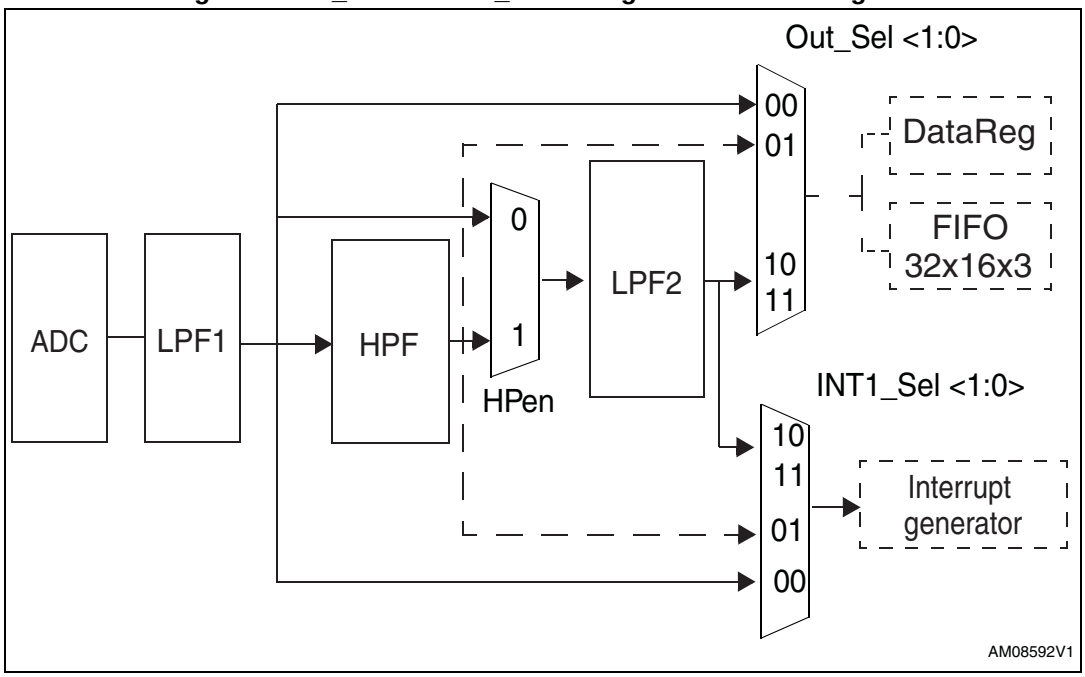
BOOT	FIFO_EN	StopOnFTH	HPen	IG_Sel1	IG_Sel0	Out_Sel1	Out_Sel0

Table 32. CTRL5 description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content(1))
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO Enable)
StopOnFTH	Sensing chain FIFO stop values memorization at FIFO Threshold. Default value: 0 0 = FIFO depth is not limited (32 digital words per axis) 1 = FIFO depth is limited to FIFO Threshold which is defined in FIFO_CTRL (2Eh Register)
HPen	High Pass filter Enable. Default value: 0 (0: HPF disabled; 1: HPF enabled see *Figure 23.*)
IG_Sel1-IG_Sel0	INT Generator selection configuration. Default value: 00 (See *Figure 23.*)
Out_Sel1-Out_-Sel0	Out selection configuration. Default value: 00 (See *Figure 23.*)

1. Boot request is executed as soon as internal oscillator is turned-on. It is possibile to set bit while in Power-down mode, in this case it will be served at the next normal mode or sleep mode.

Figure 23. IG_Sel and Out_Sel configuration block diagram



7.7 REFERENCE (25h)

Table 33. REFERENCE register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0

Table 34. REFERENCE register description

Ref 7-Ref0	Digital high pass filter reference value. Default value: 0

7.8 OUT_TEMP (26h)

Table 35. OUT_TEMP register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0

Table 36. OUT_TEMP register description

Temp7-Temp0	Temperature data (-1LSB/deg with 8 bit resolution). The value is expressed as two's complement.

7.9 STATUS (27h)

Table 37. STATUS register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA

Table 38. STATUS description

ZYXOR	X, Y, Z -axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data has overwritten the previous one before it was read)
ZOR	Z axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the Z-axis has overwritten the previous one)
YOR	Y axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the Y-axis has overwritten the previous one)
XOR	X axis data overrun. Default value: 0 (0: no overrun has occurred; 1: a new data for the X-axis has overwritten the previous one)
ZYXDA	X, Y, Z -axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z axis new data available. Default value: 0 (0: a new data for the Z-axis is not yet available; 1: a new data for the Z-axis is available)
YDA	Y axis new data available. Default value: 0 (0: a new data for the Y-axis is not yet available;1: a new data for the Y-axis is available)
XDA	X axis new data available. Default value: 0 (0: a new data for the X-axis is not yet available; 1: a new data for the X-axis is available)

7.10 OUT_X_L (28h), OUT_X_H (29h)

X-axis angular rate data. The value is expressed as two’s complement.

7.11 OUT_Y_L (2Ah), OUT_Y_H (2Bh)

Y-axis angular rate data. The value is expressed as two’s complement.

7.12 OUT_Z_L (2Ch), OUT_Z_H (2Dh)

Z-axis angular rate data. The value is expressed as two’s complement.

7.13 FIFO_CTRL (2Eh)

Table 39. FIFO_CTRL register

FM2	FM1	FM0	FTH4	FTH3	FTH2	FTH1	FTH0

Table 40. FIFO_CTRL register description

FM2-FM0	FIFO mode selection. Default value: 000 (see *Table 41*)
FTH4-FTH0	FIFO threshold setting. Default value: 0

Table 41. FIFO mode configuration

FM2	FM1	FM0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-stream mode
1	1	0	Dynamic stream mode
1	1	1	Bypass-to-FIFO mode

7.14 FIFO_SRC (2Fh)

Table 42. FIFO_SRC register

FTH	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0

Table 43. FIFO_SRC register description

FTH	FIFO threshold status. (0: FIFO filling is lower than FTH level; 1: FIFO filling is equal or higher than FTH level)
OVRN	Overrun bit status. (0: FIFO is not completely filled; 1:FIFO is completely filled)
EMPTY	FIFO empty bit. (0: FIFO not empty; 1: FIFO empty)
FSS4-FSS0	FIFO stored data level of the unread samples

7.15 IG_CFG (30h)

Table 44. IG_CFG register

AND/OR	LIR	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE

Table 45. IG_CFG description

AND/OR	AND/OR combination of Interrupt events. Default value: 0 (0: OR combination of interrupt events 1: AND combination of interrupt events
LIR	Latch Interrupt Request. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched) Cleared by reading IG_SRC reg.
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured angular rate value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured angular rate value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured angular rate value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured angular rate value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured angular rate value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured angular rate value lower than preset threshold)

Configuration register for Interrupt source.

7.16 IG_SRC (31h)

Table 46. IG_SRC register

0	IA	ZH	ZL	YH	YL	XH	XL

Table 47. IG_SRC description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z High event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z Low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y High event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y Low event has occurred)

Table 47. IG_SRC description

XH	X high. Default value: 0 (0: no interrupt, 1: X High event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X Low event has occurred)

Interrupt source register. Read only register.

Reading at this address clears IG_SRC IA bit (and eventually the interrupt signal on INT1 pin) and allows the refresh of data in the IG_SRC register if the latched option was chosen.

7.17 IG_THS_XH (32h)

Table 48. IG_THS_XH register

DCRM	THSX14	THSX13	THSX12	THSX11	THSX10	THSX9	THSX8

Table 49. IG_THS_XH description

DCRM	Interrupt generation counter mode selection. Default value: 0 0 = Reset 1 = Decrement
THSX14 - THSX8	Interrupt threshold on X axis. Default value: 000 0000

7.18 IG_THS_XL (33h)

Table 50. IG_THS_XL register

THSX7	THSX6	THSX5	THSX4	THSX3	THSX2	THSX1	THSX0

Table 51. IG_THS_XL description

THSX7 - THSX0	Interrupt threshold on X axis. Default value: 0000 0000

7.19 IG_THS_YH (34h)

Table 52. IG_THS_YH register

-	THSY14	THSY13	THSY12	THSY11	THSY10	THSY9	THSY8

Table 53. IG_THS_YH description

THSY14 - THSY8	Interrupt threshold on Y axis. Default value: 000 0000

7.20 IG_THS_YL (35h)

Table 54. IG_THS_YL register

THSY7	THSY6	THSY5	THSY4	THSY3	THSY2	THSY1	THSY0

Table 55. IG_THS_YL description

THSY7 - THSY0	Interrupt threshold on Y axis. Default value: 0000 0000

7.21 IG_THS_ZH (36h)

Table 56. IG_THS_ZH register

-	THSZ14	THSZ13	THSZ12	THSZ11	THSZ10	THSZ9	THSZ8

Table 57. IG_THS_ZH description

THSZ14 - THSZ8	Interrupt threshold on Z axis. Default value: 000 0000

7.22 IG_THS_ZL (37h)

Table 58. IG_THS_ZL register

THSZ7	THSZ6	THSZ5	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0

Table 59. IG_THS_ZL description

THSZ7 - THSZ0	Interrupt threshold on Z axis. Default value: 0000 0000

7.23 IG_DURATION (38h)

Table 60. IG_DURATION register

WAIT	D6	D5	D4	D3	D2	D1	D0

Table 61. IG_DURATION description

WAIT	WAIT enable. Default value: 0 (0: disable; 1: enable)
D6 - D0	Duration value. Default value: 000 0000

D6 - D0 bits set the minimum duration of the Interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

WAIT bit has the following meaning:

Wait ='0': the interrupt falls immediately if signal crosses the selected threshold

Wait ='1': if signal crosses the selected threshold, the interrupt falls after a number of samples equal to the duration counter register value.

Figure 24. Wait disabled

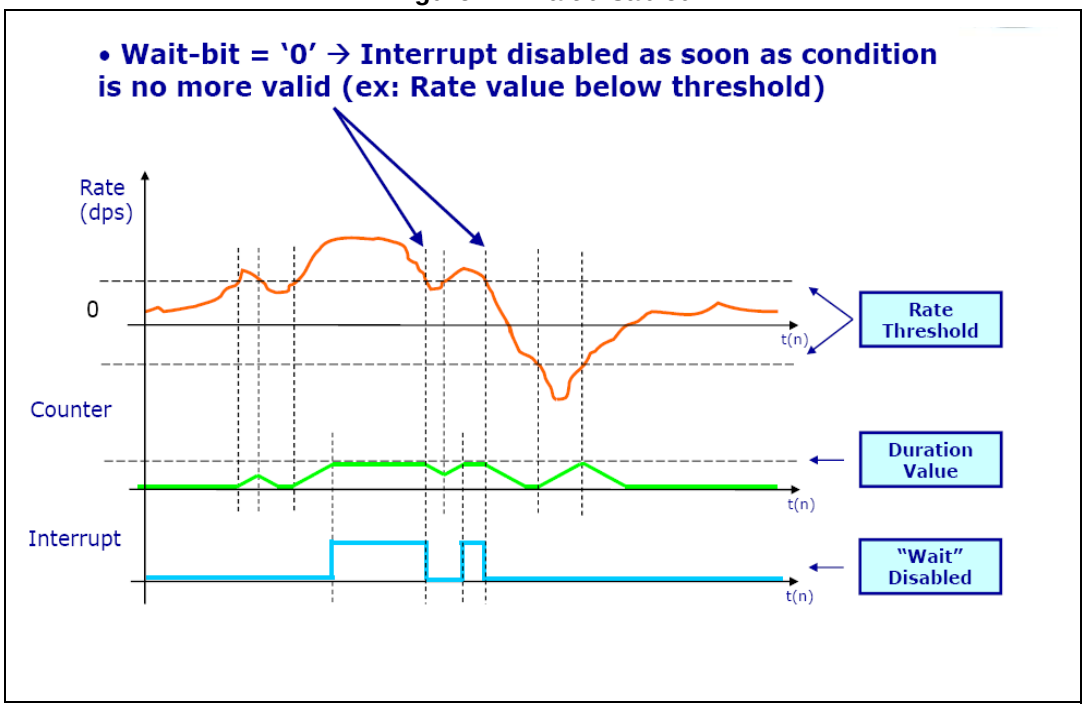
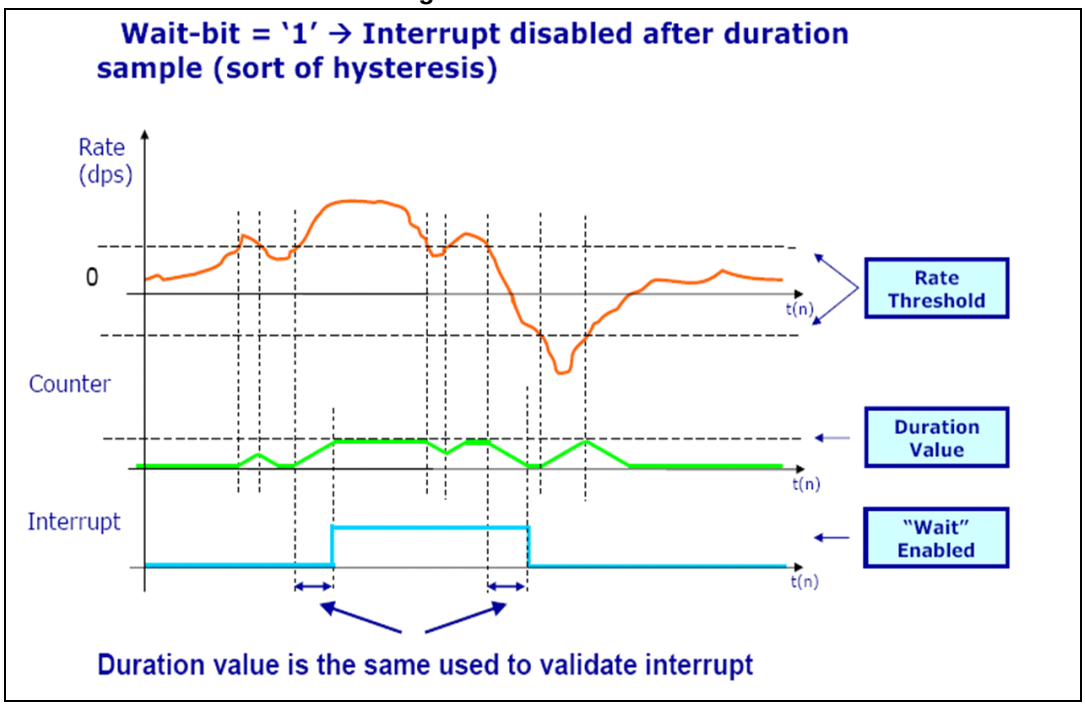


Figure 25. Wait enabled



7.24 LOW_ODR (39h)

Table 62. LOW_ODR register

--	--	DRDY_HL	0(1)	I2C_dis	SW_RES	0(1)	Low_ODR

1. These bits must be set to '0' for proper working of the device.

Table 63. LOW_ODR description

DRDY_HL	DRDY/INT2 pin active level. Default value: 0 0 = DRDY active high 1 = DRDY active low
I2C_dis	0 = both the I2C and SPI interfaces enabled (default) 1 = SPI only
SW_RES	Software reset. Default value: 0 0 = Normal Mode 1 = Reset Device (this bit is cleared by hardware after next flash boot)
Low_ODR	Low speed ODR. Default value: 0 Refer to *Table 21* DR and BW configuration setting: for ODR and Bandwidth configuration on CTRL1 register 0 = Low Speed ODR disabled 1 = Low Speed ODR enabled

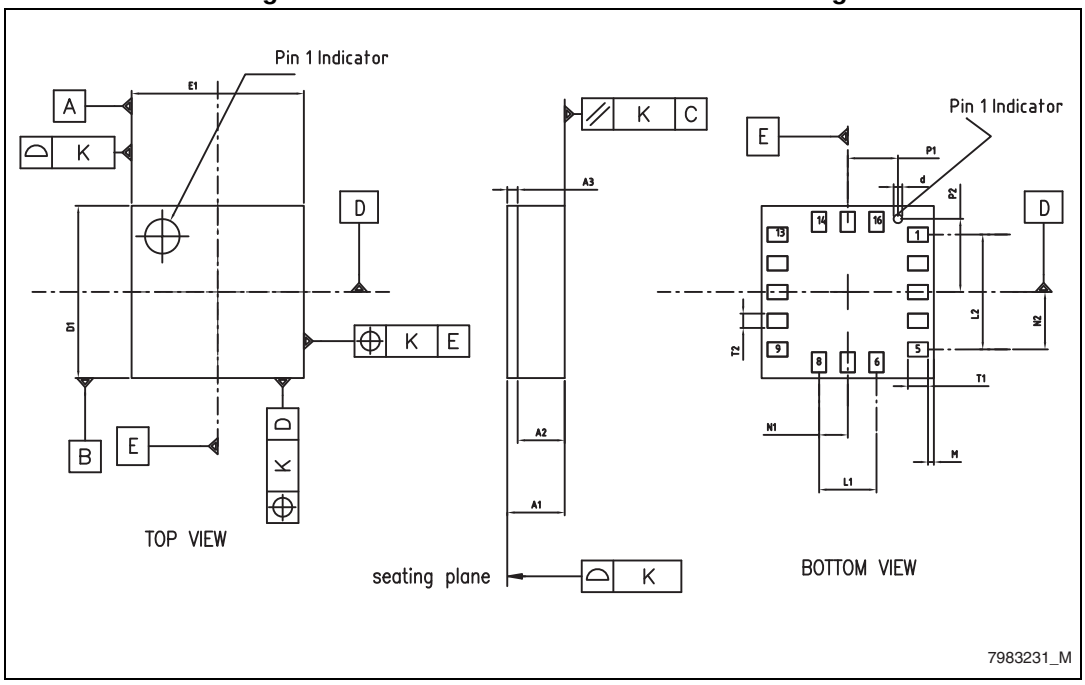
8 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 64. LGA 3x3x1.0 16L mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A1			1
A2		0.785	
A3		0.200	
D1	2.850	3.000	3.150
E1	2.850	3.000	3.150
L1		1.000	1.060
L2		2.000	2.060
N1		0.500	
N2		1.000	
M	0.040	0.100	
P1		0.875	
P2		1.275	
T1	0.290	0.350	0.410
T2	0.190	0.250	0.310
d		0.150	
k		0.050	

Figure 26. LGA 3x3x1.0 16L mechanical drawing



9 Revision history

Table 65. Document revision history

Date	Revision	Changes
20-Jul-2012	1	Initial release.
05-Mar-2013	2	Added *Chapter 3: Application hints*, *Chapter 6: Output register mapping* and *Chapter 7: Register description* Updated *Chapter 4.2: FIFO*.

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