

ST(意法) STMAV340TTR PDF

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STMAV340

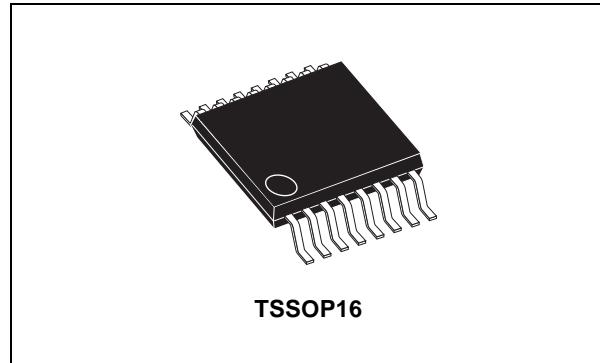
Low ON Resistance Quad, SPDT, Wide-Bandwidth Video Switch

Features

- Bi-directional operation
- 4 input/output channels analog video switch
- Wide bandwidth 300MHz
- Low 4Ω switch resistance between two ports
- Excellent R_{ON} matching between channels
- Minimal propagation delay through the switch
- Low quiescent current consumption
- V_{CC} Operating Range: 4.0V to 5.5V
- Zero bounce in flow-through mode
- Control inputs compatible with TTL level
- All input/output pins are on the same side facilitates PCB routing
- Data and control inputs provide the undershoot clamp diode
- Guaranteed break-before-make timing
- High ESD rating: > 2kV HBM
- -40°C to 85°C operating temperature range
- Suitable for both RGB and Composite-Video Switching
- Available in a small TSSOP16 package

Applications

- Advanced TVs
- Front projectors
- LCD Monitors
- Notebook PCs
- DVD Players



Description

The STMAV340 is a bidirectional quad (4 channel), high speed single pole/double throw (SPDT), low power CMOS TTL-compatible analog video switch designed for advanced video applications which demand superior image quality. The low ON Resistance (R_{ON}) of the switch allows inputs to be connected to outputs without adding propagation delay or generating additional ground bounce noise.

STMAV340 is designed for very low cross-talk, low bit-to-bit skew, high channel-to-channel noise isolation, and low I/O capacitance. The switch offers very little or practically no attenuation of the high speed signals at the outputs, thus preserving the signal integrity enough to pass stringent requirements.

The STMAV340 is able to simplify the PCB routing on inputs and outputs as well as reduce the overall BOM costs by eliminating the need for more costly input-output controllers.

Order Codes

Part Number	Temperature Range	Package	Comments
STMAV340	-40°C to $+85^{\circ}\text{C}$	TSSOP16	STMAV340TTR

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1 Summary Description

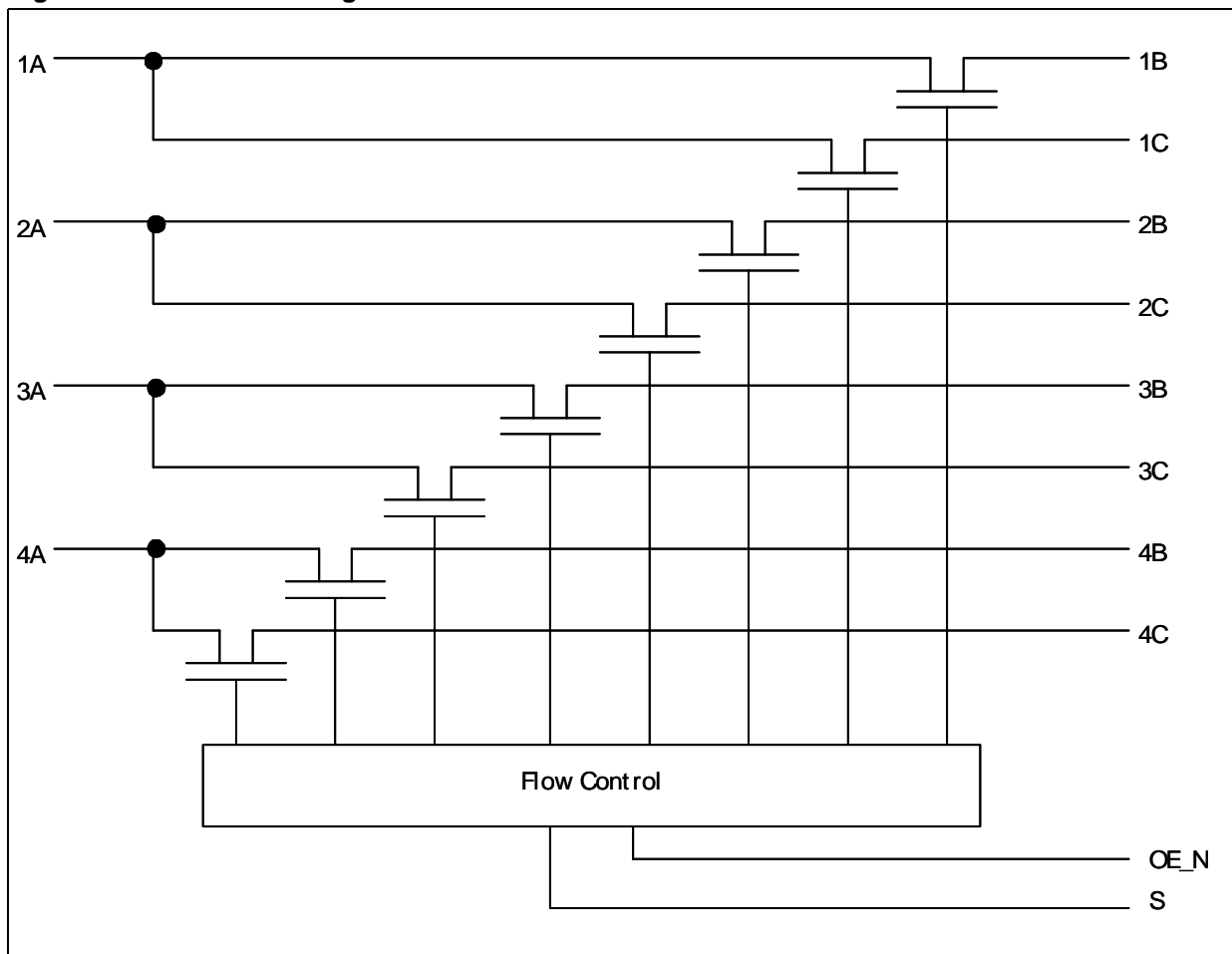
1.1 Functional Description

The STMAV340 is a high bandwidth, analog video switch. It is low ON-resistance and low I/O capacitance result in a very small propagation delay.

When OE_N is set to LOW, the select (S) pin connects port A to the selected port B or port C output. When OE_N is set to HIGH, the switch is OPEN and a high-impedance state exists between the A port and B/C ports.

Low differential gain and phase make this switch ideal for component and RGB video applications. This device has high bandwidth and low crosstalk, making it ideal for high frequency applications as well.

Figure 1. Functional Diagram



2 Pin Configuration

Figure 2. Pin Configuration (Top View)

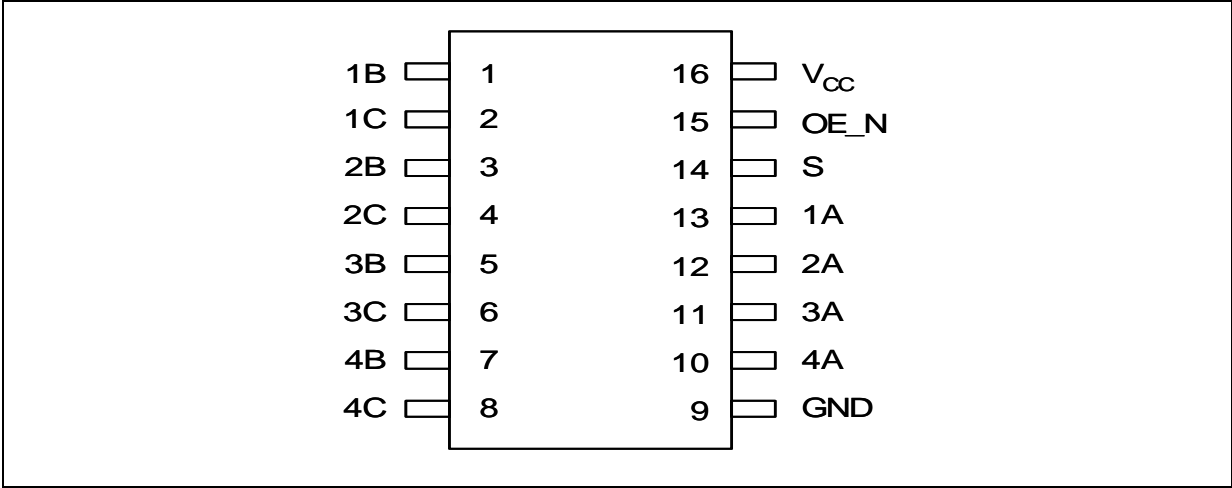


Table 1. Pin Description

Symbol	Type	Name and Functions
OE_N	IN	Bus Switch Enable Note: 1
S	IN	Select Input
1A ,2A ,3A ,4A	IN/OUT	Port A; Analog Video I/Os
1B ,2B ,3B ,4B	IN/OUT	Bus B; Analog Video I/Os
1C, 2C, 3C, 4C	IN/OUT	Bus C; Analog Video I/Os
V _{CC}		Power supply
GND		Ground

Note: 1 Tie to V_{CC} through a pull-up resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver.

Table 2. Truth Table

OE_N	S	ON Switch
0	0	1B,2B,3B,4B
0	1	1C,2C,3C,4C
1	X	Disabled

3 Application Diagrams

Figure 3. STMAV340 2-to-1 Analog Video Switch Used in an LCD TV

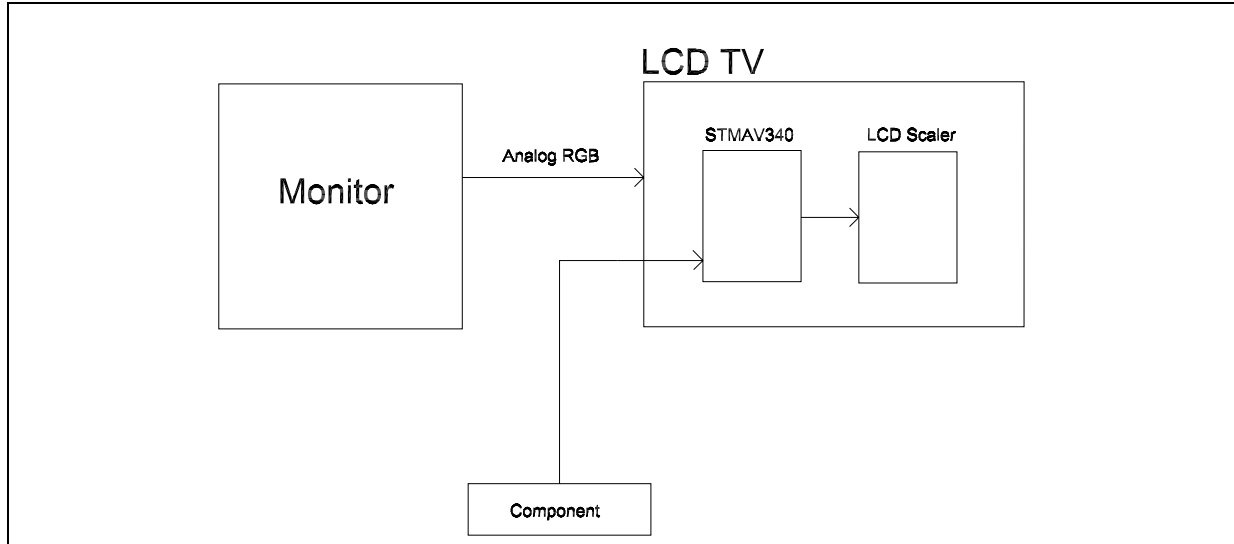
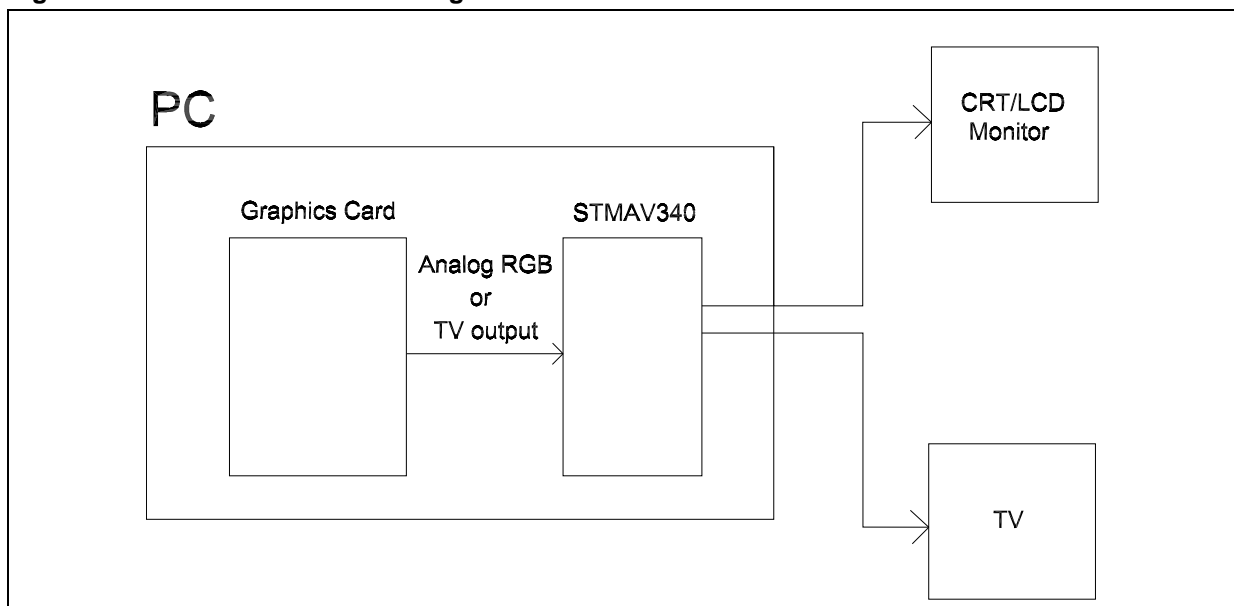


Figure 4. STMAV340 1-to-2 Analog Video Switch Used in a PC



3.1 Power Supply Sequencing

Proper power-supply sequencing is advised for all CMOS devices. Applying V_{CC} before sending any signals to the input/output or control pins is recommended.

4 Maximum Ratings

Stressing the device above the rating listed in the “Absolute Maximum Ratings” table may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the Operating sections of this specification is not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 3. Absolute Maximum Ratings

$T_A = 25^{\circ}\text{C}$, GND= 0V

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage to Ground	-0.5 to + 7.0	V
V_S	DC Switch Voltage	-0.5 to + 7.0	V
V_{IN}	DC Input Voltage	-0.5 to + 7.0	V
I_{IK}	DC Input Diode Current	-50	mA
I_{OUT}	DC Output Sink Current	128	mA
I_{CC}/I_{GND}	DC V_{CC} /GND Current	± 100	mA
T_{STG}	Storage Temperature Range	-65 to 150	$^{\circ}\text{C}$

Note: Absolute maximum ratings are those values above which damage to the device may occur. Functional operation under these conditions is not implied. All voltages are referenced to GND.

5 Electrical Characteristics

Table 4. Recommended Operating Conditions

$T_A = -20$ to $+70^\circ\text{C}$

Symbol	Parameter (<i>Note: 1</i>)	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Power Supply Voltage		4.0		5.5	V
V_{IN}	Input Voltage		0		5.5	V
V_{OUT}	Output Voltage		0		5.5	V
t_r, t_f	Input Rise and Fall Time	Switch Control Input	0		5	ns/V
		Switch I/O	0		DC	ns/V
T_A	Free Air Operating Temperature		-40		+85	$^\circ\text{C}$
V_{ESD}	ESD-Human Body Model (HMB) <i>Note: 1</i>		-2		+2	kV

Note: 1 Unused control inputs must be held HIGH or LOW. They should not float.

2 In accordance with IEC61000-4-2, level 4

Table 5. DC Electrical Characteristics

$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$

Symbol	Parameter	Test Conditions	$V_{CC}(\text{V})$	Min.	Typ.	Max.	Unit
	Analog Signal Range		5	0		2.0	V
V_{IK}	Clamp Diode Voltage	$I_{IN} = -18\text{mA}$	4.5			-1.2	V
V_{IH}	HIGH Level Input Voltage		4.0-5.5	2.0			V
V_{IL}	LOW Level Input Voltage		4.0-5.5			0.8	V
I_I	Input Leakage Current	$0 \leq V_{IN} \leq 5.5\text{V}$	5.5			± 10	μA
I_{OFF}	OFF-STATE Leakage Current	$0 \leq A, B \leq V_{CC}, C \leq V_{CC}$	5.5			± 10	μA
R_{ON}	Switch ON resistance (<i>1</i>)	$V_{IN} = 1.0\text{V}, I_{ON} = 13\text{mA}$	4.5		3	7	Ω
		$V_{IN} = 2.0\text{V}, I_{ON} = 26\text{mA}$	4.5		7	10	Ω
I_{CC}	Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND, $I_{OUT} = 0$	5.5			3	μA
ΔI_{CC}	Increase in I_{CC} per Input	One input at 3.4V Other inputs at V_{CC} or GND	5.5			2.5	mA

Note: 1 Measured by the voltage drop between pin A and B/C pins at the indicated current through the switch. ON Resistance is determined by the lower of the voltages on the two (A or B/C) pins.

Table 6. AC Electrical Characteristics $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $C_L = 20\text{pF}$, $R_U = R_D = 75\Omega$

Symbol	Parameter	Test conditions	$V_{CC} = 4.5 - 5.5\text{V}$			$V_{CC} = 4.0\text{V}$		Unit
			Min.	Typ.	Max.	Min.	Max.	
t_{PZH} , t_{PZL}	Output Enable Time, Select to Bus B/C	$V_I = 7\text{V}$ for t_{PZL}			5.2		5.7	ns
	Output Enable Time, OE_N to Bus A, B/C	$V_I = \text{OPEN}$ for t_{PHZ}			5.1		5.6	ns
t_{PHZ} , t_{PLZ}	Output Disable Time, Select to Bus B/C	$V_I = 7\text{V}$ for t_{PLZ}			5.2		5.5	ns
	Output Disable Time, Output Enable time OE_N to Bus A, B/C	$V_I = \text{OPEN}$ for t_{PHZ}			5.5		5.5	ns
B_W	-3dB Bandwidth	$R_L = 150\Omega$ $T_A = 25^{\circ}\text{C}$	300					MHz
X_{TALK}	Crosstalk	$R_{IN} = 10\Omega$ $R_L = 150\Omega$, 10 MHz		-58				dB
D_G	Differential Gain	$R_L = 150\Omega$ $f = 3.58\text{ MHz}$		0.64				%
D_P	Differential Phase	$R_L = 150\Omega$ $f = 3.58\text{ MHz}$		0.1				Deg.
P_{IRR}	Off Isolation	$R_L = 150\Omega$ 10 MHz		-60				dB

Table 7. Capacitance

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Control Pin Input Capacitance	$V_{CC} = 5.0\text{V}$		3		pF
$C_{I/O}$	Input/Output Capacitance A Port	V_{CC}		7		pF
	Input/Output Capacitance B/C Port	$OE_N = 5.0\text{V}$		5		pF
C_{ON}	Switch On Capacitance	$V_{CC} = 5.0\text{V}$, $OE_N = 0.0\text{V}$		12		pF

6 Test Circuit and Diagrams

Note: C_L includes probe and jig capacitance.

All input pulses are supplied by generators having the following characteristics: $PRR = 10\text{MHz}$,
 $Z_0 = 50\Omega$, $t_r, t_f = 2.5\text{ns}$.

Figure 5. AC Test Circuit

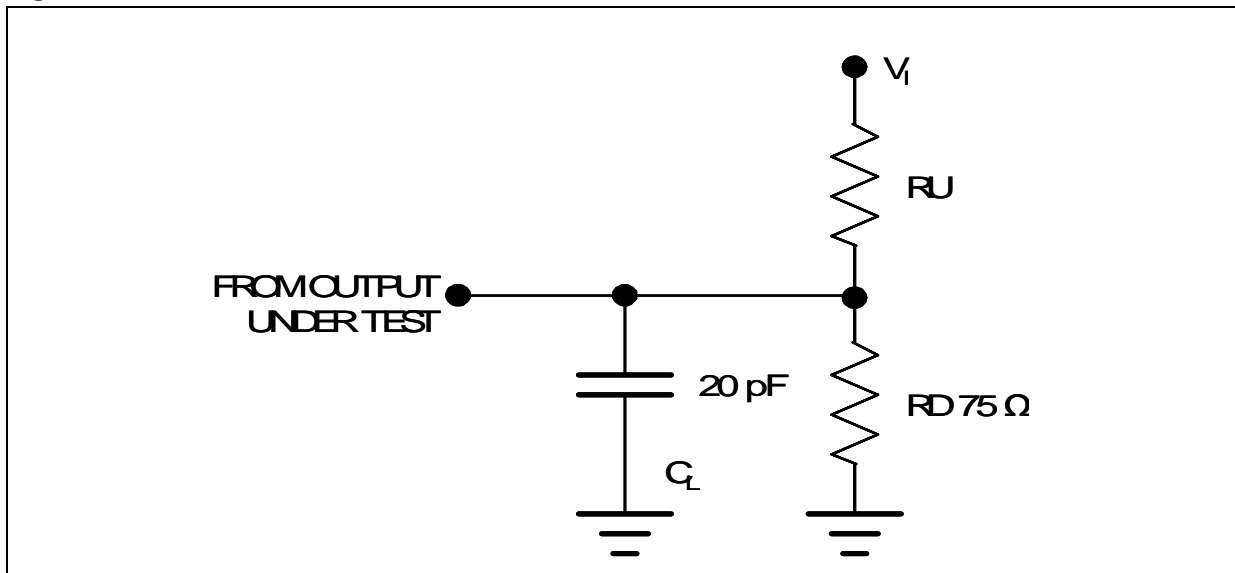


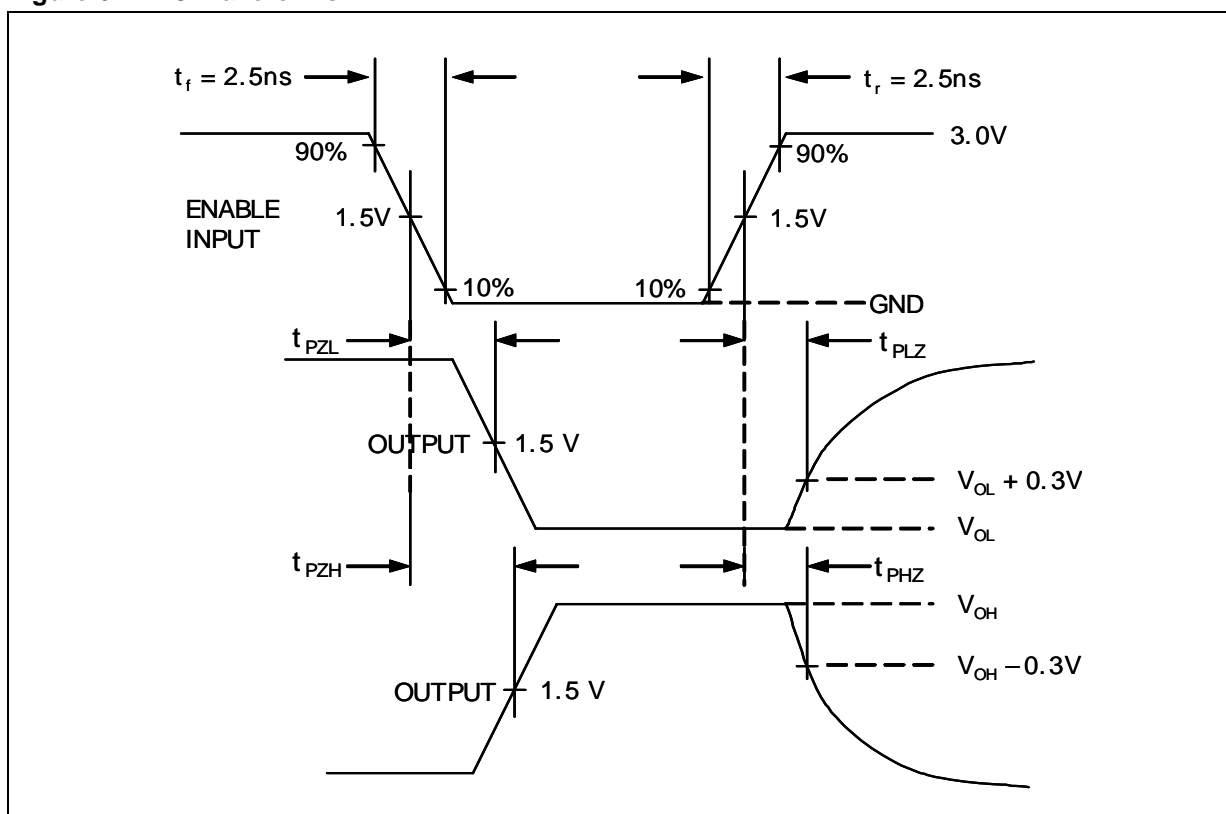
Figure 6. AC Waveforms

Figure 7. ON Resistance Test Circuit

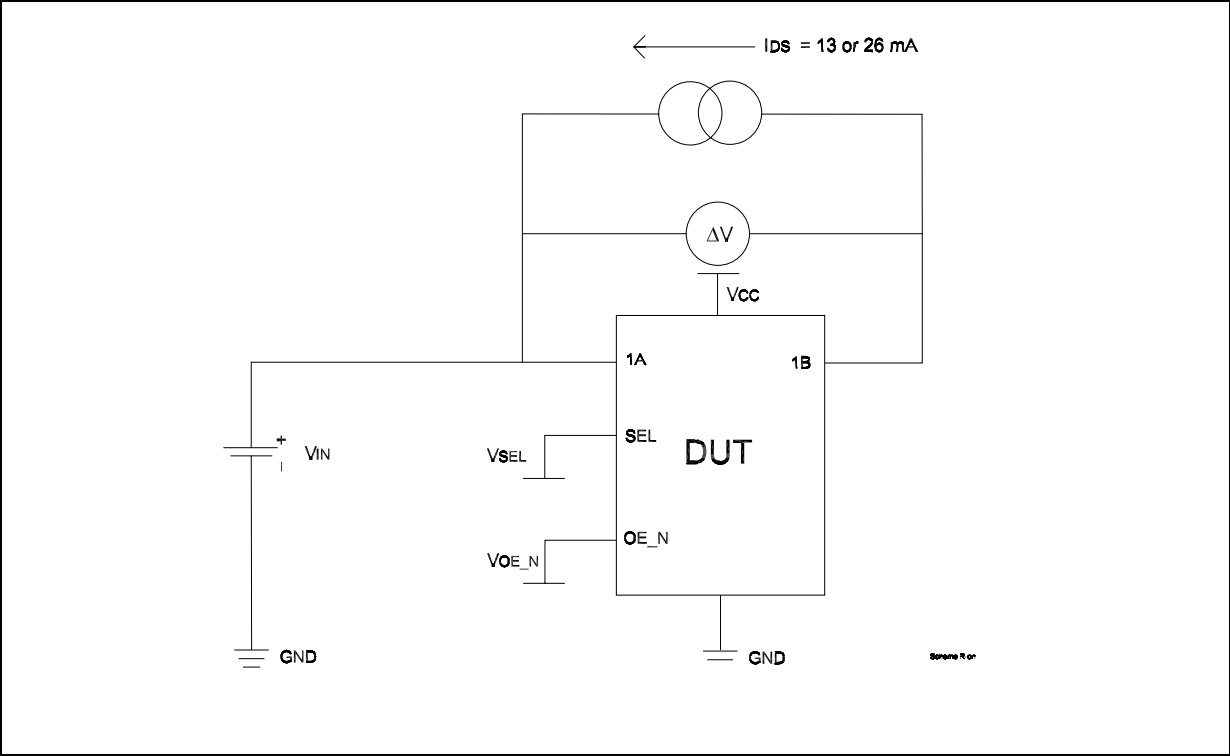
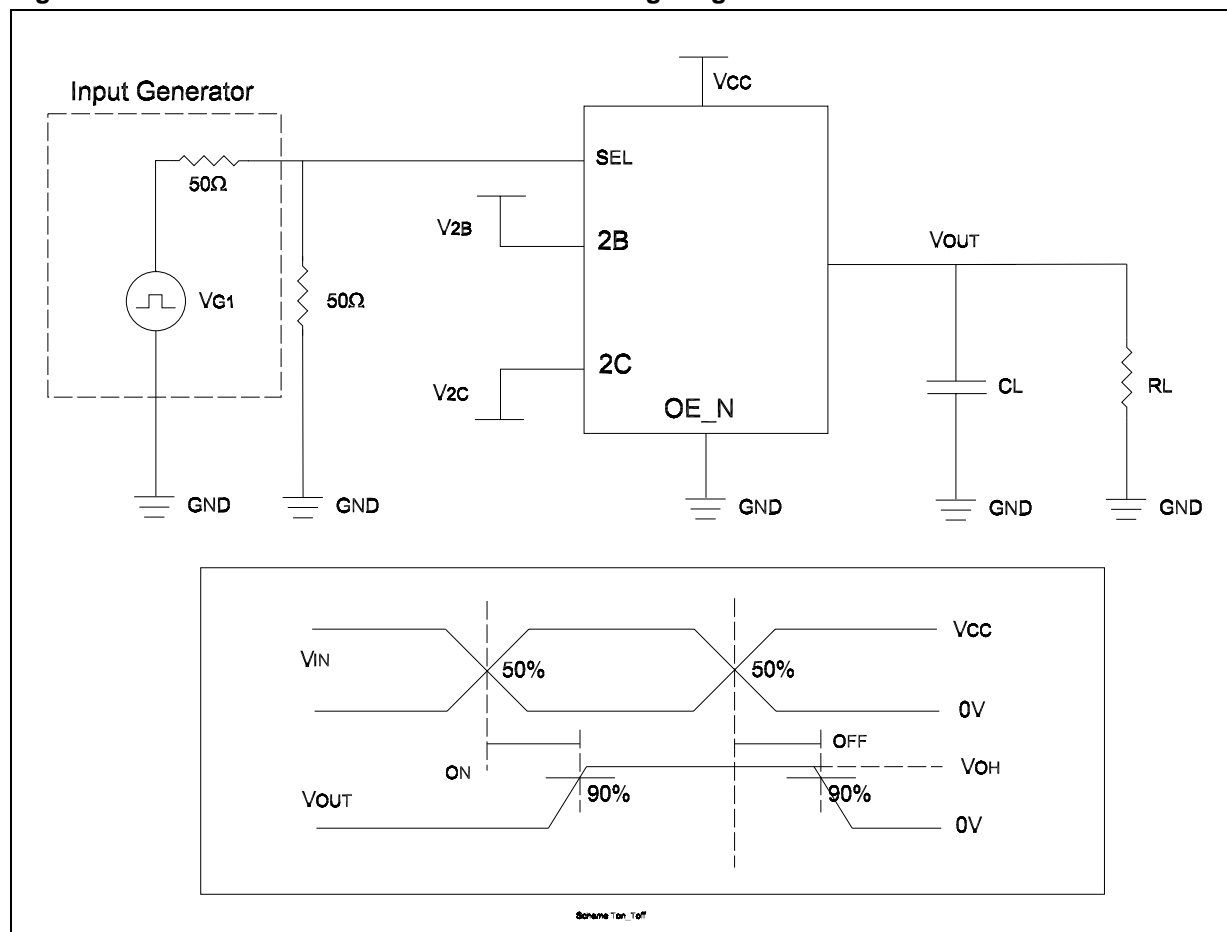


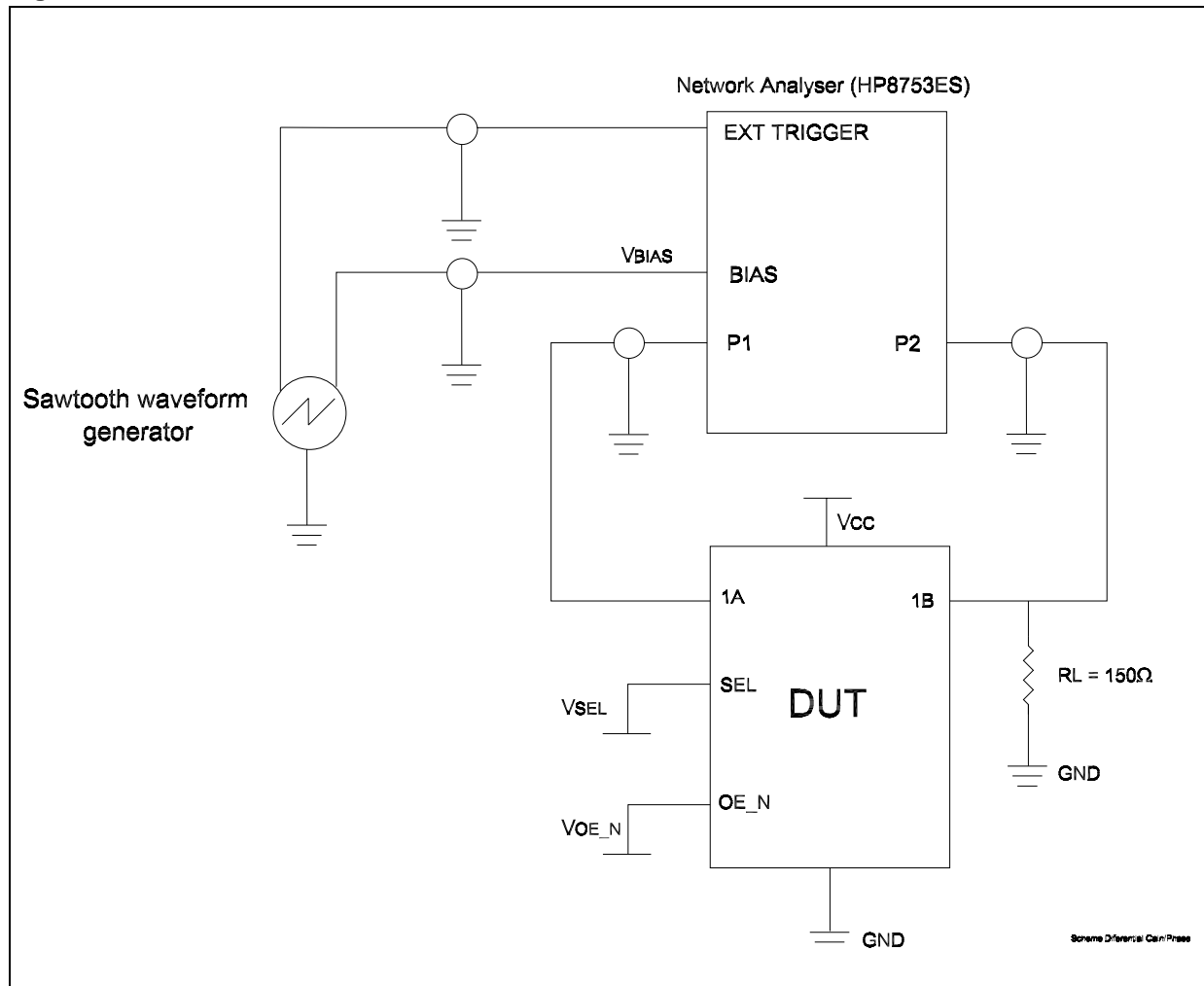
Table 8. Test Circuit

Test	V _{CC}	R _L	C _L	V _{2B}	V _{2C}
t _{ON}	4.75V ± 0.75V	75	20	GND	V _{CC}
	4.75V ± 0.75V	75	20	V _{CC}	GND
t _{OFF}	4.75V ± 0.75V	75	20	GND	V _{CC}
	4.75V ± 0.75V	75	20	V _{CC}	GND

Figure 8. Turn-on/Turn-off Test Circuit and Timing Diagram

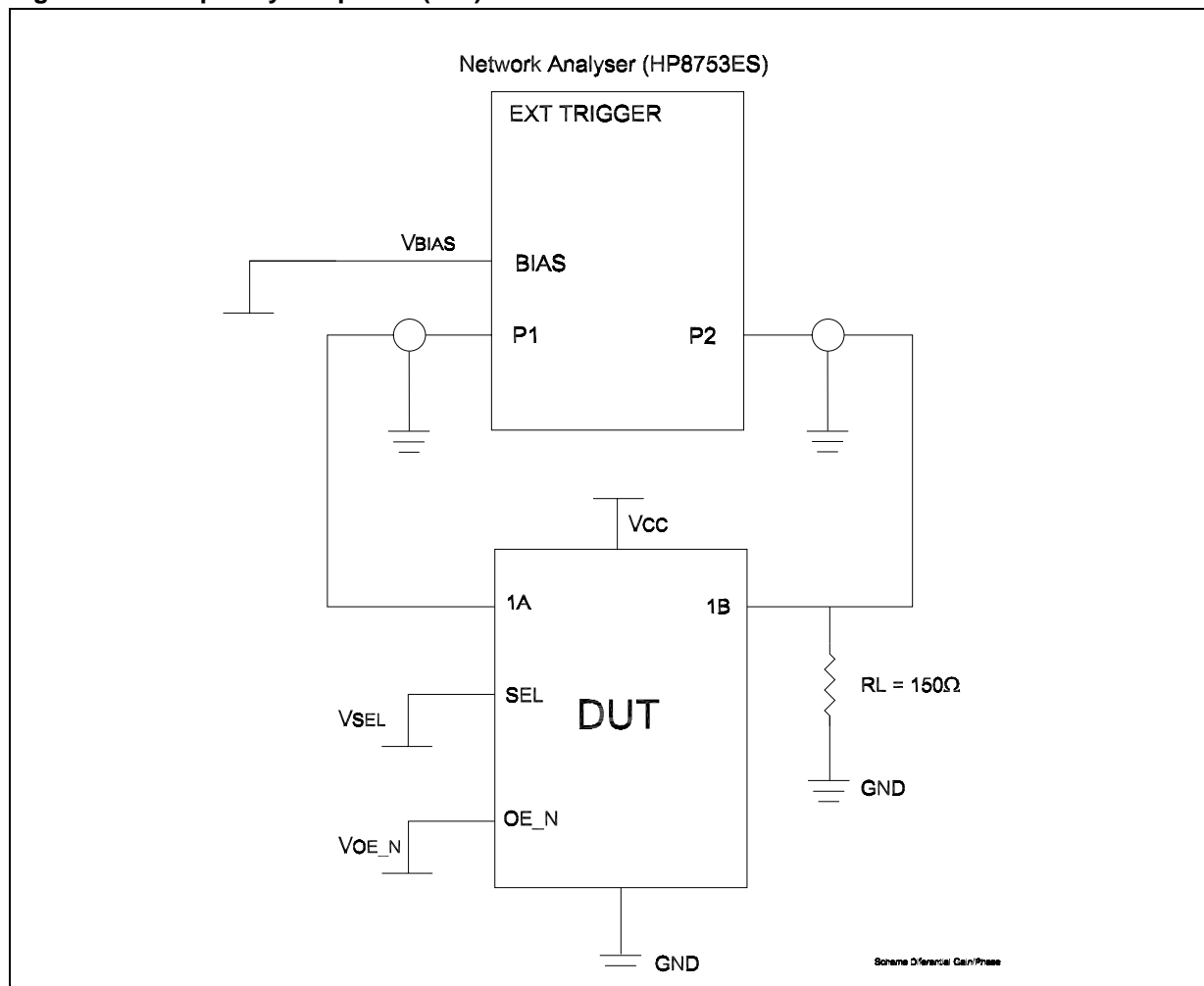
Differential gain and phase are measured at the output of the ON channel. For example, when $V_{SEL} = 0$, $V_{OE_N} = 0$ and 1A is the input, the output is measured at 1B.

Figure 9. Differential Gain/Phase Measurement Test Circuit



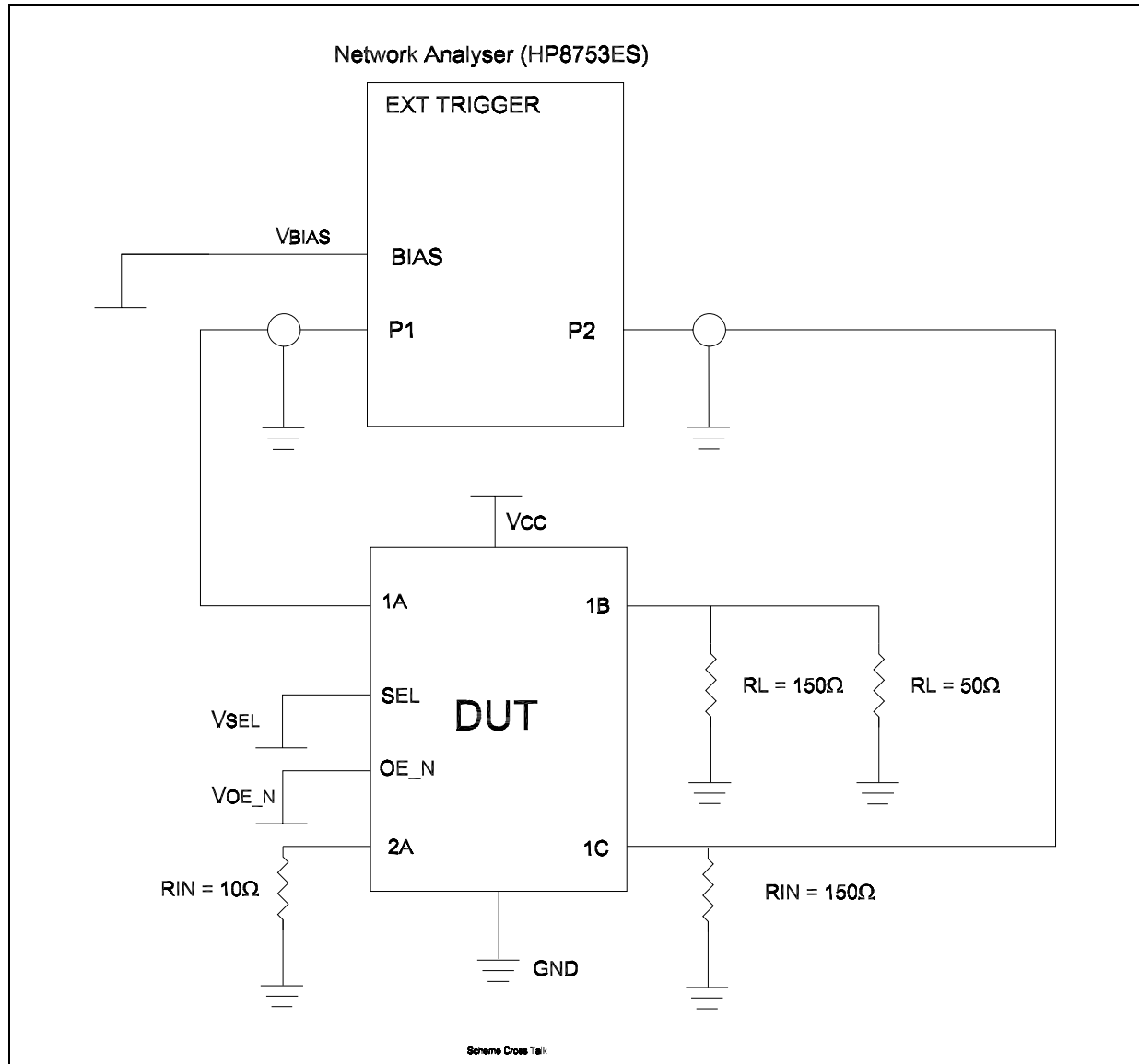
Frequency response is measured at the output of the ON channel. For example, when $V_{SEL} = 0$, $V_{OE_N} = 0$ and 1A is the input, the output is measured at 1B. All unused analog I/O ports are left open.

Figure 10. Frequency Response (BW) Test Circuit



A 50Ω termination resistor is needed for the network analyzer. Crosstalk is measured at the output of the non-adjacent ON channel. For example, $V_{SEL} = 0$, $V_{OE_N} = 0$, and 1A is the input, the output is measured at 1C. All unused analog input ports are connected to GND through IO-ports and the output ports are connected to GND through the 50Ω pull down resistors.

Figure 11. Crosstalk Test Circuit



A 50Ω termination resistor is needed for the network analyzer. Off-isolation is measured at the output of the OFF channel. For example, when $V_{SEL} = V_{CC}$, $V_{OE_N} = 0$ and 1A is the input, the output is measured at 1B. All unused analog input ports are left open, and the output ports are connected to GND through the 50Ω pulldown resistors.

Figure 12. Off-Isolation Test Circuit

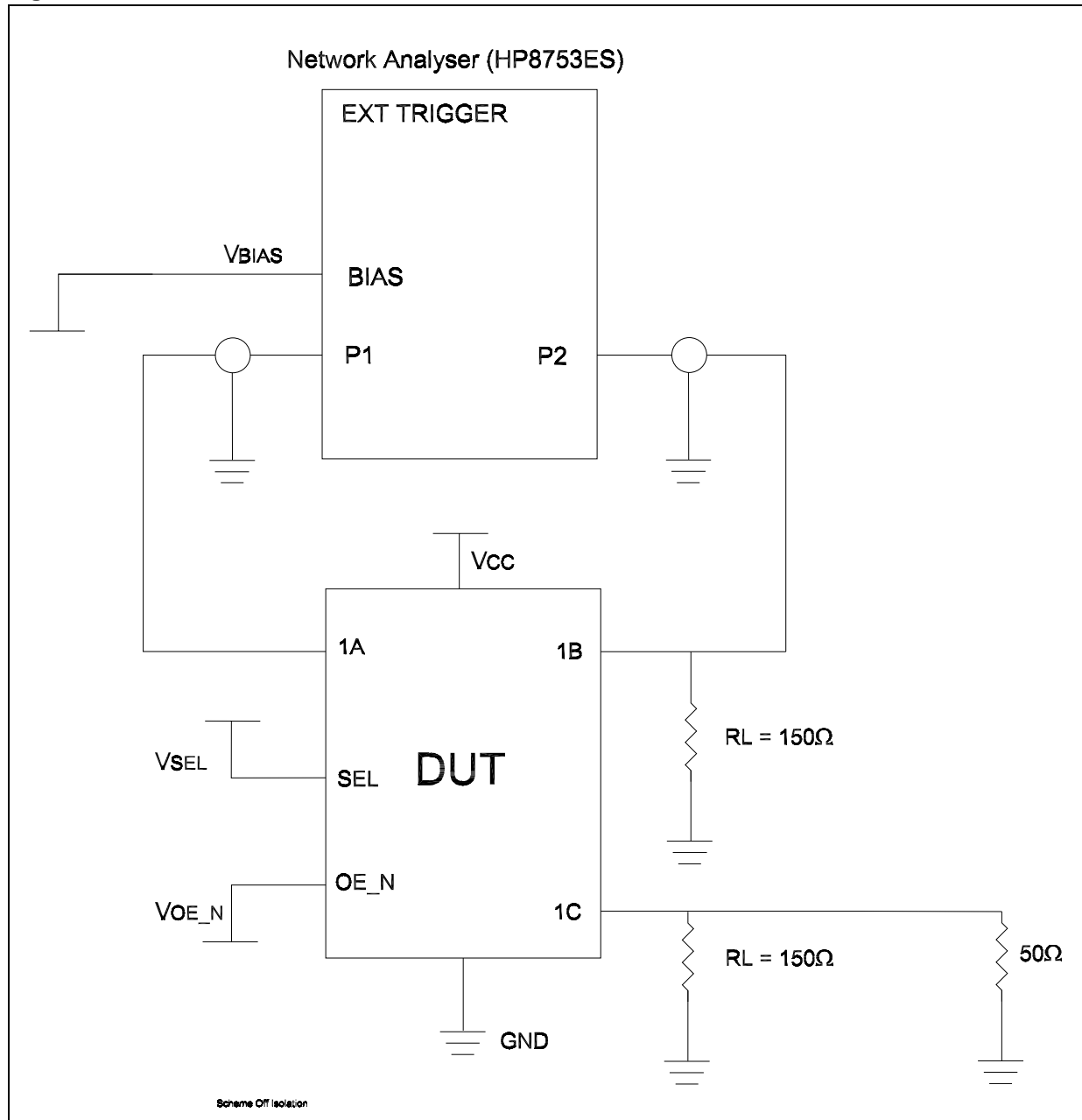


Figure 13. I/O Pin (Input Side) ESD Protection Circuit

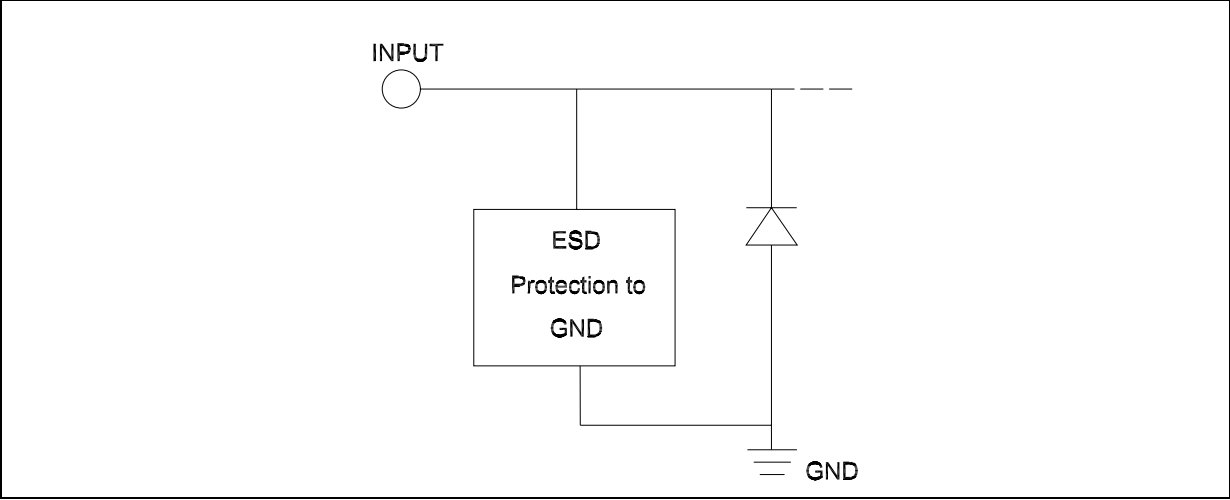


Figure 14. I/O Pin (Output Side) ESD Protection Circuit

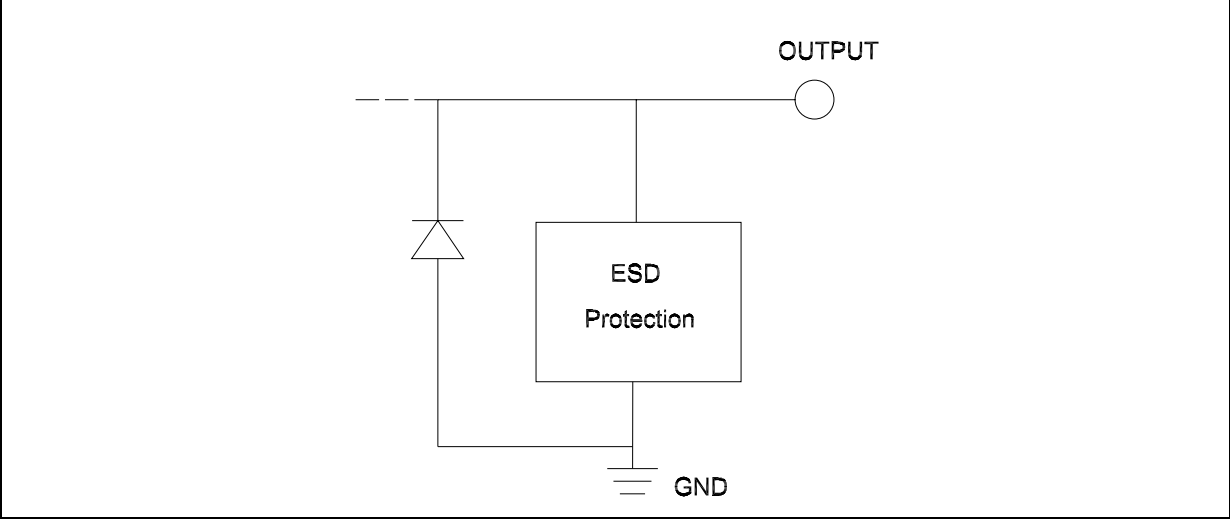
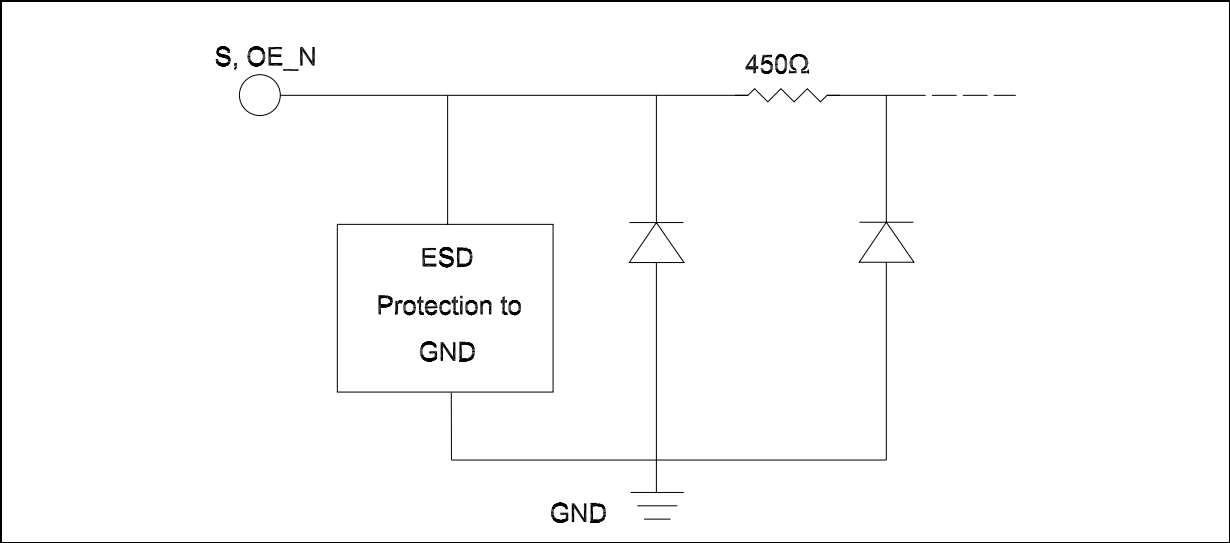


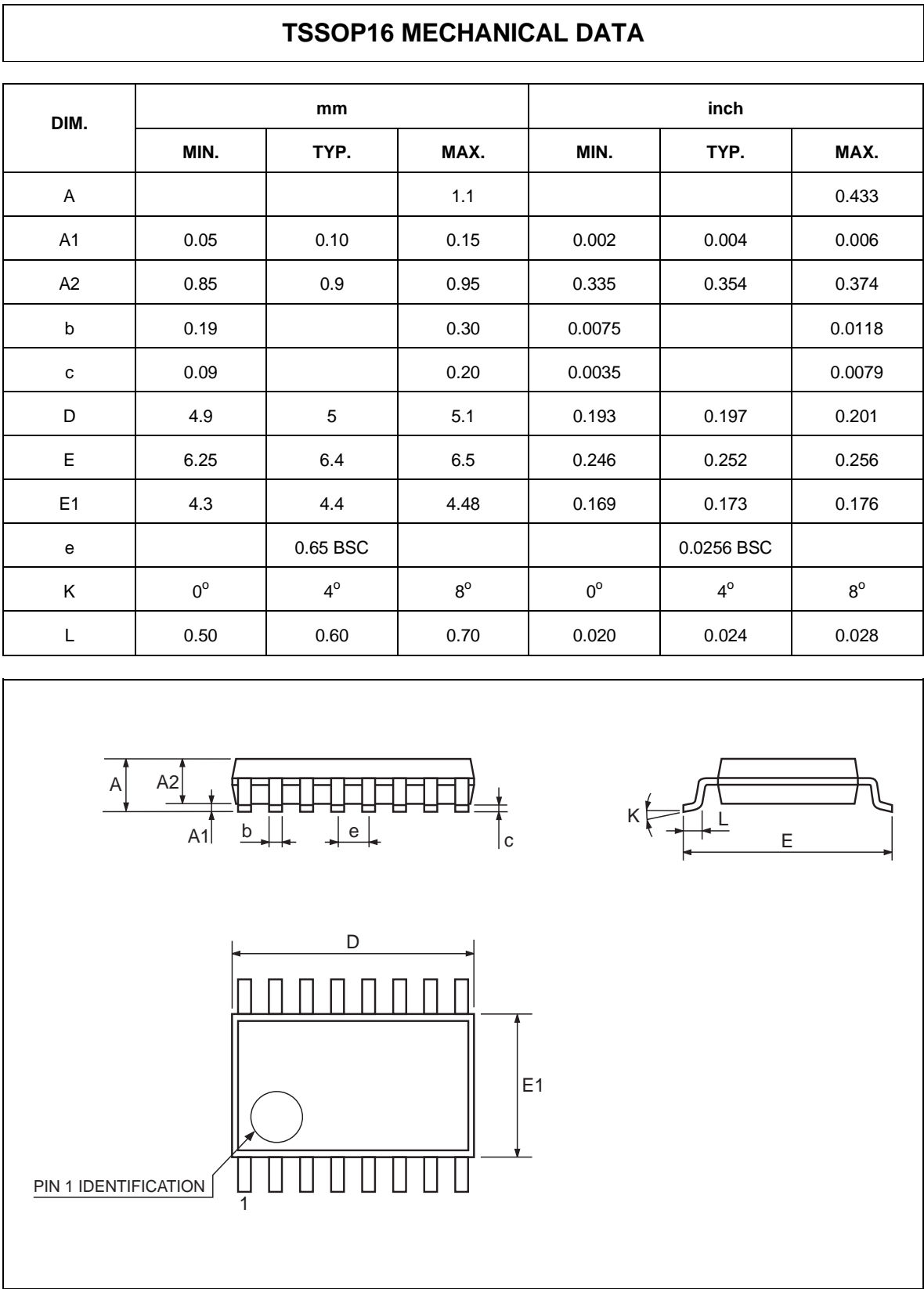
Figure 15. S and OE_N Input ESD Protection Circuit



7 Package Mechanical Data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second Level Interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com.

Figure 16. TSSOP16 Mechanical Data



8 Revision History

Date	Revision	Description of Change
09-Sep-2005	1	First issue

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